Field-Effect Transistor Based on Si with $LaAlO_{3-\delta}$ as the Source and Drain *

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N-type $LaAlO_{3-\delta}$ thin films are epitaxially grown on p-type Si substrates. An enhancement mode field-effect transistor is constructed with oxygen deficient $LaAlO_{3-\delta}$ as the source and drain, p-type Si as the semiconducting channel, and SiO_2 as the gate insulator, respectively. The typical current-voltage behavior with field-effect transistor characteristic is observed. The ON/OFF ratio reaches 14 at a gate voltage of 10 V, the field-effect mobility is 10 cm^2/V·s at a gate voltage of 2 V, and the transconductance is 5×10^{-6} A/V at a drain-source voltage of 0.8 V at room temperature. The present field-effect transistor device demonstrates the possibility of realizing the integration of multifunctional perovskite oxides and the conventional Si semiconductor.

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Heterostructures consisting of perovskite oxide materials exhibit the richness of functional properties, such as ferroelectricity, colossal magnetoresistance, optical properties and others, due to the intrinsic properties of perovskite oxides and the interface effects.[1−9] There is a considerable effort to epitaxially grow perovskite oxide films on Si substrates because this can link up the functional properties of perovskite oxide and the conventional Si semiconductor.[10−14] We have epitaxially grown $SrTiO_3$,[15] $BaTiO_3$,[16] $La_{0.7}Sr_{0.3}MnO_3$,[17] and $LaAlO_3$ [18] films on Si substrates and observed the photoelectric characteristics and the hysteresis current-voltage characteristics. However, it is still a big challenge to fabricate real functional devices based on perovskite oxide and a Si semiconductor. It is known that electronics technology depends on the availability of satisfactory amplifiers. Since the simplest and possibly the most direct way would be a device in which the conductance of a channel is modified through an electrostatic field, the field-effect transistor (FET) came into being. It has been widely used as a primary element in integrated circuits and electronic devices. The general principle of FET is modifying the current flow in a conductor by means of an electrostatic field. Furthermore, applying the FET principle to perovskite materials provides attractive prospects, and investigations on such a device can be very helpful for understanding the electronic states of heterointerfaces.[19,20] So far as we know, only very limited FETs based on perovskite oxides have been reported[20−23] and no FET based on Si with perovskite oxides as source and drain has been reported. In this study, an enhancement mode FET is fabricated with n-type $LaAlO_{3-\delta}$ (LAO) as the source and drain, p-type Si as the semiconducting channel, and SiO_2 as the gate insulator (LAO-Si FET). The typical current-voltage behavior with FET characteristic is observed in the LAO-Si FET.

In order to fabricate the LAO-Si FET, we epitaxially grew LAO thin films on p-type Si substrates by the laser molecular beam epitaxy technique. A p-type Si (100) wafer was dipped into HF (4%) solution for 40 s after wet-chemical cleaning, so as to remove the native oxide and to form a hydrogen-terminated surface. Then the treated substrate was immediately delivered into the epitaxial chamber. An LAO layer with a thickness of 100 nm was epitaxially grown on the p-type Si (100) substrate with resistivity of 12.95 Ω·cm under the oxygen pressure of 2×10^{-4} Pa. The growth process of the LAO thin film was monitored by *in-situ* reflection high energy electron diffraction (RHEED), and the crystalline structure of LAO film was tested by x-ray diffraction (XRD). The measurements of RHEED and XRD show that the LAO film was single phased and epitaxially grown on the Si substrate. The Hall coefficient measurement confirmed that the LAO film is electron conductive and the resistivity is 1.3×10^{-2} Ω·cm at room temperature.

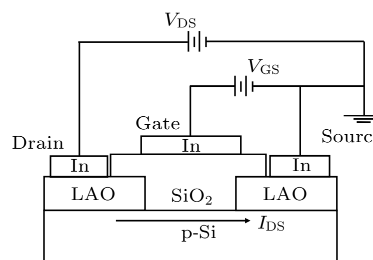

Fig. 1. Schematic diagram of LAO-Si FET structure.

Figure 1 shows a schematic diagram of LAO-Si FET. First, the LAO layer on the Si substrate was notched to form a groove so that the LAO film was divided into two regions as the source and drain. Then,

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a 300 nm amorphous SiO_2 layer was grown on the sample by plasma enhanced chemical vapor deposition (PECVD) as the gate insulator, and the electrode contact between the source and drain was formed by etching the SiO_2 onto the LAO layer. Finally, indium electrodes were painted on the source, drain and the top of the gate insulator SiO_2, respectively, to form an n-channel enhancement mode n-p-n FET. A typical size for the LAO-Si FET device is 1 mm ×2 mm. The channel length L of the device was about 20 µm and the width W was 1 mm.

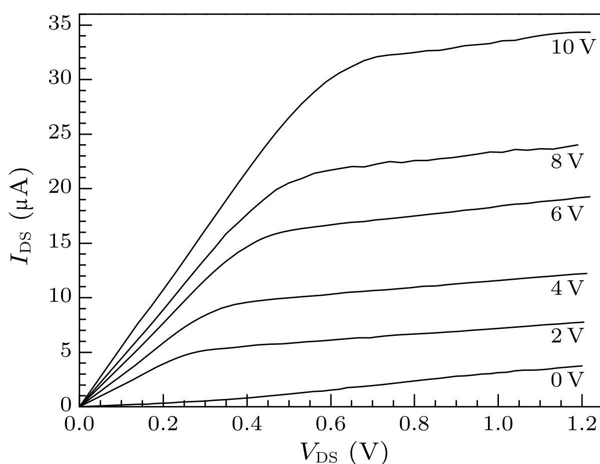

Fig. 2. Drain-source $I_{DS} - V_{DS}$ curves of LAO-Si FET under various gate voltages V_{GS}.

A well-behaved output characteristic was observed from the LAO-Si FET. Figure 2 shows the drain-source current-voltage ($I_{DS} - V_{DS}$) curves under various gate voltages V_{GS} measured at room temperature. Although there is a small leakage current when $V_{GS} = 0$ V, the drain-source current I_{DS} is enhanced under the positive gate voltages V_{GS}, and there is almost no current flowing from source to drain at negative V_{GS}. This phenomenon is a typical n-channel enhancement-mode FET behavior. It can be seen from Fig. 2 that, at small V_{DS}, the $I_{DS} - V_{DS}$ curves are linear, with a slope proportional to V_{GS}. When V_{DS} increases and respectively approaches 0.3 V at $V_{GS} = 2$ V, 0.4 V at $V_{GS} = 4$ V, 0.5 V at $V_{GS} = 6$ V, 0.6 V at $V_{GS} = 8$ V, and 0.7 V at $V_{GS} = 10$ V, a distinct saturation of I_{DS} (pinch-off) can be observed.

Similar to the conventional Si semiconductor FETs, the enhancement of I_{DS} is due to the accumulation of negative carriers at the interface between the SiO_2 insulator and the Si substrate under the positive gate voltages V_{GS}, as shown in Fig. 3(a). The saturation of I_{DS} indicates that, at higher V_{DS}, the density of carriers induced near the drain electrode gets depleted to zero. Although the undepleted length of the channel filled with free carriers becomes shorter, its resistance does not change because of the contingent lower carrier density. The carriers in the depleted region of the channel are all swept into the drain by the longitudinal drain-source electric field. Therefore, the $I_{DS} - V_{DS}$ curves become those of saturation. As shown in Fig. 3(b), the channel was depleted and the channel resistance was so large that the source and the drain were isolated when $V_{GS} < 0$. In this case, we believe that the main reason to bring the leakage current for the LAO-Si FET is the presence of some impurities introduced into the films during the complex device fabrication process.

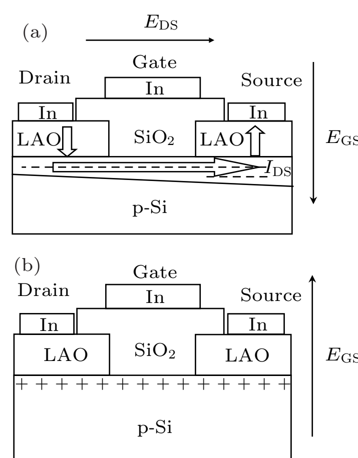

Fig. 3. (a) Schematic diagram of the formation of n-type conducting channel under positive gate voltages V_{GS}. (b) Schematic diagram of the formation of the interface depletion layer under negative gate voltages V_{GS}.

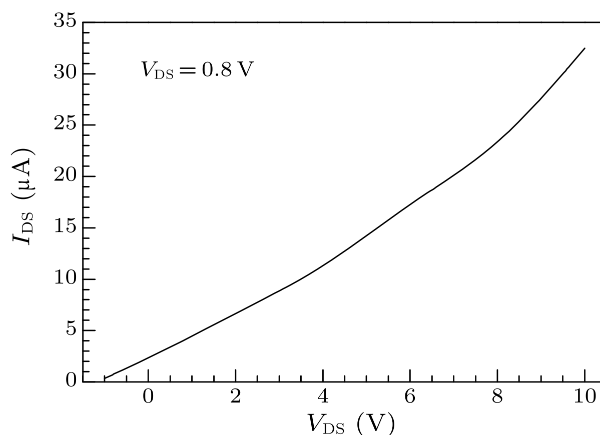

Fig. 4. Transfer characteristic of LAO-Si FET at $V_{DS} = 0.8$ V.

The transfer characteristic of the device at $V_{DS} = 0.8$ V is plotted in Fig. 4. I_{DS} increases almost linearly with V_{DS}. The transconductance g is defined as

$$g = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}}, \tag{1}$$

we can obtain $g = 5 \times 10^{-6}$ A/V at $V_{DS} = 0.8$ V. It can be expected that g can be further improved by optimizing the fabrication process and increasing the carrier mobility μ of the channel.

The ratio of I_{DS} at a given V_{GS} to that for zero gate bias is defined as the ON/OFF ratio. From Fig. 2,

we can obtain the ON/OFF ratios of 7.5 and 14 with $V_{\rm GS} = 6\,{\rm V}$ and $10\,{\rm V}$, respectively, at $V_{\rm DS} = 0.8\,{\rm V}$.

As for conventional FET, when the drain-source current $I_{\rm DS}$ in the channel is saturated, i.e., the channel region is in the pinch-off state, the field-effect mobility $\mu_{\rm sat}$ can be expressed as

$$\mu_{\rm sat} = \left(\frac{\partial\sqrt{I_{\rm DS}}}{\partial V_{\rm GS}}\right)^2 \frac{2L}{C_i W}, \tag{2}$$

where C_i is the capacitance per unit area of the SiO_2 gate insulator measured to be $0.8\,{\rm nF/cm^2}$ in the present device.

The carrier saturation mobility $\mu_{\rm sat}$ can be obtained from Fig. 4 by using Eq. (2). We can find that the mobility $\mu_{\rm sat}$ decreases with increasing $V_{\rm GS}$. The saturation mobility $\mu_{\rm sat}$ is $10\,{\rm cm^2/V{\cdot}s}$ at $V_{\rm GS} = 2\,{\rm V}$, $8\,{\rm cm^2/V{\cdot}s}$ at $V_{\rm GS} = 4\,{\rm V}$, and to $6\,{\rm cm^2/V{\cdot}s}$ at $V_{\rm GS} = 6\,{\rm V}$, respectively. Though the mobility $\mu_{\rm sat}$ of LAO-Si FET presented here is lower than those of the conventional Si FETs, it is higher than those of FETs based on all perovskite oxides.[21–23]

In summary, an enhancement mode FET based on Si with LAO as the source and drain has been fabricated successfully and a well-behaved transistor characteristic has been observed. The present LAO-Si FET links up the perovskite oxide and the conventional Si semiconductor and demonstrates the possibility of realizing the integration of multifunctional perovskite oxides and the conventional Si semiconductor. Further investigations, such as replacing LAO by a functional perovskite oxide, and improving the fabrication process to enhance the carrier mobility, are being planned.

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