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High resistance modulation by the electric field based on $La_{0.9}Sr_{0.1}MnO_3/SrTiO_3/Si$ structure

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A field-effect configuration based on $La_{0.9}Sr_{0.1}MnO_3/SrTiO_3/Si$ structure is fabricated on Si substrate by laser molecular-beam epitaxy. The resistance modulation by electric field of the $La_{0.9}Sr_{0.1}MnO_3/SrTiO_3/Si$ structure is investigated in detail. An evident resistance modulation effect is observed at 80 K. The channel resistance modulation by field effect reaches 1.4×10^7% and 2.6×10^6% when V_{DS} are –2 and –6.5 V, respectively. The ON/OFF ratio of approximately 4000 is obtained. The present results are worthy of further investigations for potential applications of resistance modulation by electrostatic field in the heterostructures consisting of perovskite oxides and Si.

field effect, perovskite oxide thin films, resistance modulation

Perovskite oxides have exotic properties, including superconductivity, ferroelectricity, ferromagnetism, colossal magnetoresistance and optical properties[1−9]. And these materials provide attractive possibilities for various multifunctional devices such as ferroelectric field effect transistor (FET)[10] and visible-blind ultraviolet photodetector[11]. Electrostatic field can not only modulate resistance but also modify the elemental electronic properties of materials[12]. Therefore, it is of great value to combine such multifunctional materials with traditional semiconductors to exploit novel properties and versatile devices[13,14]. Pallecchi et al.[15] have reported a $SrTiO_3$-based FET, but which does not show typical transistor behavior. They also mentioned that they had tried perovskite oxides as drain and source, but the devices show the electrical shorts between source and drain or Schottky contacts with the channel layer.

In our work, we fabricate a field effect configuration based on $La_{0.9}Sr_{0.1}MnO_3/SrTiO_3/Si$ structure with insulating $SrTiO_3$ (STO) as gate and semi-conductive $La_{0.9}Sr_{0.1}MnO_3$ (LSMO) as source and drain. STO has a high dielectric constant and is usually considered as a good candidate as gate insulator to replace SiO_2 in FETs in the future[16−18]. As shown in Figure 1, the STO channel layer in our device is at the top, and LSMO film on the channel layer is patterned to act as source and drain. The distance between the source and drain is ~20 μm. We investigate the resistance modulation effects of electric field in our structure. The structure exhibits a high resistance modulation by electric field at 80 K.

The LSMO and STO layers are prepared by a computer-controlled laser molecular-beam epitaxy system equipped with *in situ* reflection high energy electron diffraction (RHEED)[19]. A single crystal p-type silicon wafer is used as the substrate. A XeCl pulsed laser with energy density of 1.5 J/cm^2 is used to deposit film onto the substrate at 2 Hz repetition rate. In order to remove the amorphous SiO_2 layer from Si, the wafer is dipped into HF (4%) solution for 30—40 s, leaving a hydrogen-terminated surface. First, a 5-nm-STO buffer layer is deposited on the Si substrate by two-step method. The deposition details of the STO buffer layer are reported

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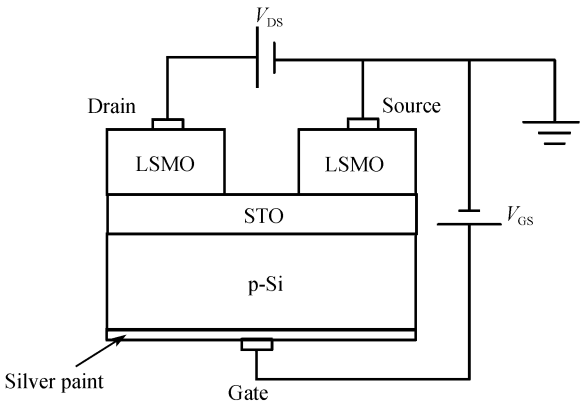

Figure 1 The schematic and measurement circuit of the LSMO/STO/p-Si field effect structure.

somewhere else[20]. Subsequently, the STO thin film is deposited at 800℃ under active oxygen ambient with the pressure of 3×10^{-1} Pa. Then LSMO film is grown on the as-deposited STO layer and patterned as source and drain. Sharp and bright RHEED patterns show that both STO and LSMO films grow epitaxially layer-by-layer on the Si substrate. The thicknesses of the STO and LSMO thin films are 255 and 370 nm, respectively. Silver paint is painted on the back of Si substrate, serving as the gate electrode, and two indium electrodes are applied on the LSMO films.

The electrical transport properties of the LSMO/STO/Si structure are measured at 80 K, as shown in Figure 2. The drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) of the structure is presented under different gate voltages (V_{GS}) ranging from –4.5 to 6 V with a step of 1.5 V. The structure in our present study is an enhancement-type FET. Under positive gate voltages V_{GS},

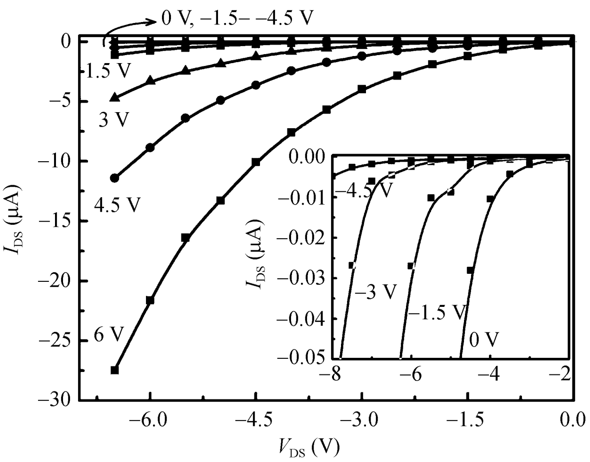

Figure 2 Drain-source current I_{DS} versus drain-source voltage V_{DS} of the LSMO/STO/Si structure for various gate voltages V_{GS} at 80 K.

the current I_{DS} increases with V_{DS} exponentially. While negative gate voltages are applied, the current I_{DS} decreases and becomes even lower than that when V_{GS} was 0. It can be seen from the inset of Figure 2 that the value of the current I_{DS} under $V_{GS} = 0$, −1.5, −3, −4.5 V are several nanoamperes or even lower. Moreover, at a fixed V_{DS}, the current I_{DS} increases with V_{GS} remarkably. This obvious field-induced effect is demonstrated as follows in terms of the variation of channel resistance with gate voltage.

Figure 3 shows the dependence of resistance R_{DS} between drain and source on the gate voltage V_{GS}, under V_{DS} being −2 and −6.5 V, respectively, in semilogarithmic plot. It can be seen from Figure 3 that, the R_{DS} almost exponentially decreases with gate voltage V_{GS} from –4.5 to +6 V when V_{DS} are –2 and –6.5 V. The channel resistance R_{DS} increases with negative gate voltages but decreases with positive gate voltages, which performs a typical p-channel transistor behavior. It is noteworthy that the channel resistance modulation, defined as $[(R_{max} - R_{min})/R_{min}]$, can reach 1.4×10^7 % and 2.6×10^6 % when V_{DS} are –2 and –6.5 V, respectively. This modulation is six and five orders of magnitude as high as that of manganite films reported by Hu et al.[21]. The ON/OFF ratio, defined as the ratio of I_{DS} at $V_{GS} = 0$ and +6 V, reaches nearly 4000 and 54 when V_{DS} are fixed at –2 and –6.5 V, respectively.

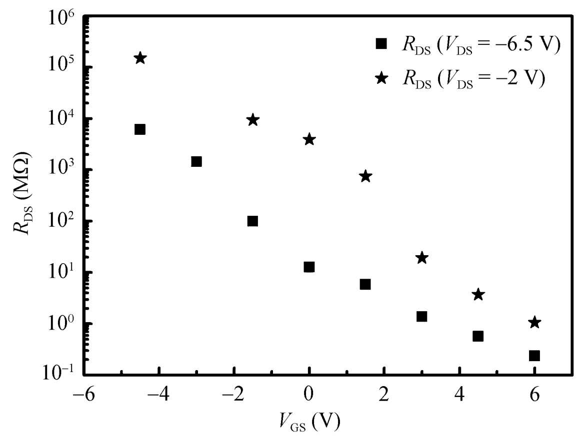

Figure 3 Channel resistance as a function of gate voltage V_{GS} at V_{DS}=–2 V and –6.5 V. The star and the square represent R_{DS} at V_{DS}=–2 V and –6.5 V, respectively.

The mechanism of the resistance modulation by electric field can be understood in the following physical picture. As shown in Figure 4(a), when positive gate voltages are applied, positive charges accumulate at the

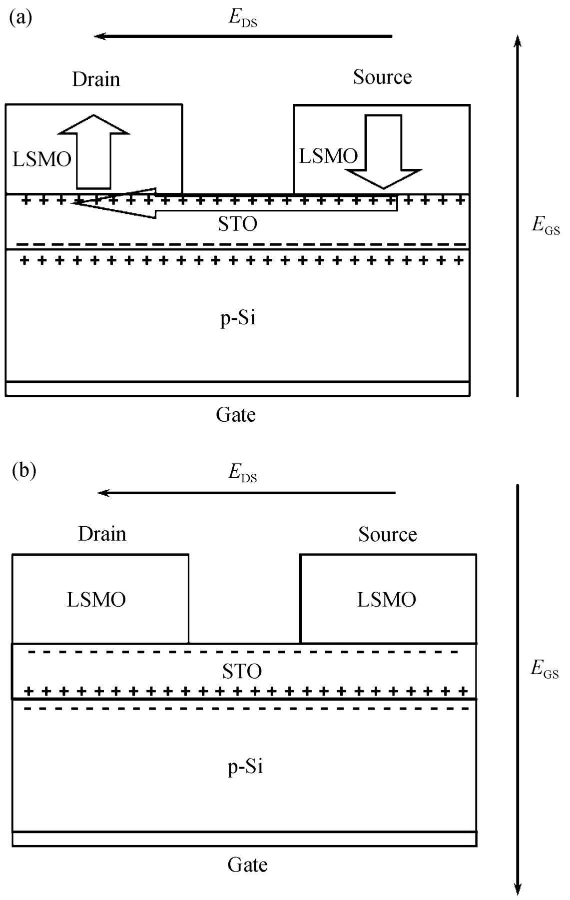

Figure 4 (a) Under positive V_{GS}, positive charges accumulated on the top of the STO layer and the channel formed; (b) under negative V_{GS}, the buildup of negative charges on the top of the STO layer depleted the positive charges while the channel could not form.

surface of STO due to the field-induced effect. Because the majority carriers of LSMO are holes, source and drain are connected by the positive charges at the top of the STO layer, so the p-type channel is formed. This results in the lower channel resistance R_{DS} and the larger current I_{DS}. When negative voltages are applied, negative charges are accumulated at the STO layer under the external electric field and isolate the source and drain, therefore the channel is depleted. The depletion of the channel causes the resistance R_{DS} to be very high and the current I_{DS} very small (Figure 4(b)).

In summary, a field effect configuration with STO as channel and LSMO as source and drain has been fabricated on Si substrate and the field effect modulation of the structure has been studied. The resistance of STO channel layer can be highly modulated by the gate voltage. When V_{DS} is –6.5 V, the channel resistance modulation can reach as high as 1.4×10^7% and 2.6×10^6% when V_{DS} are –2 and –6.5 V, respectively. And when V_{DS} is fixed at –2 V, the ON/OFF ratio can reach nearly 4000. The fabrication of a field effect structure based on growing perovskite oxide thin films on conventional semiconductors might open up the possibilities in the future generation microelectronic devices. Moreover, further investigations, both experimental and theoretical, on the mechanism of the multifunctional properties of electricity and magnetism in such systems are ongoing.

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