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Dual-Gated MoS_2 Transistors for Synaptic and Programmable Logic Functions

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Neuromorphic computers, which can store information and compute at the same time, have been considered to be a potential candidate for greatly improving computing efficiency. The development of high-performance artificial synapses, which are the basic unit of brain-like chips, is very important for realizing efficient neuromorphic computing. Here, a dual-gated MoS_2 transistor is designed to realize synaptic functions and programmable logic operations. The channel conductance is modulated via top electrolyte gating to mimic important synaptic functions, such as excitatory postsynaptic current, paired-pulse facilitation, and spike-timing dependent plasticity. The synaptic transistor exhibits ultra-low energy consumption with 12.7 fJ. Furthermore, the MoS_2 transistor can dynamically reconfigure the logic operations of "AND," "OR," and "NOT" by combining top electrolyte gating with back gating. Classical Pavlov's dog experiment can be simulated by the dual gated device. These results indicate that the proposed synaptic transistor has potential applications in realizing neuromorphic and programmable logic devices.

1. Introduction

Artificial intelligence (AI) is a branch of computer science that can do a lot of the complex work usually requiring human intelligence. Currently, the majority of AI applications are based on von Neumann machines. However, with the rapid development of AI, the von Neumann AI structure has faced huge challenges in terms of large-scale integration and consequently the high energy consumption.[1] Inspired by the brain, the emerging non-von Neumann AI structure based on neuromorphic computing has been proposed.[2] Due to the distributed storage and parallel computing, the neuromorphic architecture is much more efficient than conventional computers in handling data from AI. This approach can solve the intense energy consumption problems. An artificial synapse is the basic unit of the new architecture, and thus many recent research works have focused on the design of artificial synapse by using the phase change,[3–5] ferroelectric domains switching,[6] conductive bridge,[7–9] electrolyte gating,[10] and other mechanisms[11,12] to emulate the biological synapse behavior.

Since the discovery of graphene, 2D van der Waals materials have been extensively studied for their intriguing physical and chemical properties. Owing to its unique layered structure which facilitates the intercalation of functional ions, the van der Waals materials have been employed to simulate the rich functionality and dynamics of synapses.[13–17] Furthermore, as the neighboring layers were combined by van der Waals forces, different 2D materials can be integrated in a designed sequence to form heterostructures. The integrated architecture provides the possibility for simulating more complex synaptic functions.[18]

From the viewpoint of device structure, artificial synapses can be generally classified into two categories: two-terminal devices and synaptic transistors. Compared to two-terminal devices, synaptic transistors can receive and process external stimuli simultaneously.[19] Moreover, synaptic transistors with several gates can integrate many presynaptic signals in one device to simulate concurrent learning and dendrites integration.[20] Taking dual-gated transistors as an example, the dual-gated architecture allows to implement local activity correlations for one gate and to achieve the global plasticity modulation for the other gate. This feature makes dual-gated synaptic transistor implement complex functions, such as neuronal plasticity modulation and higher order temporal correlations.[18,21] It is worth noting that the two gates of the dual-gated transistors can also be regarded as two input terminals to realize the logic operations.[22,23] With the additional modulatory gate, the primary logic function (OR and AND) can be achieved in a single

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transistor, which can increase the integrated circuit density, but these volatile logic transistors can't store the assigned function.[21,24,25] Compared to the volatile reconfigurable logic gate, the nonvolatile reconfigurable logic gate is more efficient in dealing with application in machine learning and data analytics. Although some nonvolatile reconfigurable logic gate based on light-gated transistor has been proposed, there are still a lot of technical problems to be solved. For example, the light source needs to be integrated into the circuit.[26,27]

Here, we demonstrated a dual-gated MoS_2 transistor to reconfigure the logic operation by combining electronic and ionic regulation modes. Furthermore, we used the ionic regulation mode to emulate various synaptic functions. The designed synapse exhibited ultralow energy consumption down to 12.7 fJ per spike, indicating its potential application. An artificial neural network consisting of the proposed synaptic transistor was simulated, and a high recognition accuracy (93.9%) for the large digits was achieved. Finally, the classical Pavlov's dog conditioning experiment was emulated, exhibiting a basic form of associative-memory in our device.

2. Results and Discussion

2.1. Electrolyte Gated MoS_2 Transistor

Figure 1a illustrates the layered structure of 2H phase molybdenum disulfide (2H-MoS_2). A single layer of MoS_2 consists of three layers of atoms, in which the Mo layer is sandwiched between two S layers. MoS_2 layers are held together by weak van der Waals forces with 0.615 nm interlayer spacing.[28] To mimic the biological synapse, a dual-gated transistor based on the 2H-MoS_2 flake with a thickness of 5.6 nm was fabricated. The 2H-MoS_2 flake was fabricated on an *n*-type silicon substrate coated with a 300 nm thick SiO_2 layer by mechanical-exfoliation, and the Au electrodes were deposited using the thermal evaporation technique. The linear *I*–*V* curve between the source and drain electrodes implies a good ohmic contact (Figure S1, Supporting Information). The thickness of the MoS_2 flake was nine layers measured by atomic force microscope (AFM) and Raman spectra (Figure S2, Supporting Information). The ionic liquid N, N-diethyl-N-(2-methoxyethyl)-N-methylammonium bis-(trifluoromethyl sulphonyl) imide (DEME-TFSI) was utilized as a dielectric layer, which covered the MoS_2 channel and the top gate electrode. The schematic of the device is illustrated in Figure 1b and Figure S2a, Supporting information shows the optical picture of the electrolyte-gated MoS_2 transistor. The top and back gate electrodes are treated as two different presynaptic terminals to modify the conductance of the channel layer, which serves as a postsynaptic terminal. The transfer curves of the MoS_2 field-effect transistor under top gating were obtained by sweeping the voltage of the back gate from –1.5 to 1.5 V and then back (Figure 1c). The device exhibited a high on/off ratio (≈10^5). The transistor under top electrolyte gating showed an anticlockwise hysteresis (AH) (Figure 1c), while the transistor under back gating showed a clockwise hysteresis (CH) (Figure S3a, Supporting Information). The AH behavior during top electrolyte gating is attributed to the migration of cations and anions in an electrolyte and its relaxation dynamics.[14] For the CH behavior during back gating, the electron trapping from the dangling Si—O bonds at the SiO_2—MoS_2 interface could be responsible for the CH loop.[29] The output curves of the electrolyte-gated transistors were measured by sweeping the V_{sd} from 0 to 1.5 V, with a fixed top gate voltage varied from –1.5 to 2.6 V (Figure 1d). This device exhibited excellent linearity at low voltages as well as good pinch-off characteristics at high voltages. The top-gated MoS_2 transistor with ionic liquid exhibits much lower pinch-off voltage compared to the back-gated MoS_2 transistor with SiO_2 (Figure S3b, Supporting Information), which is due to the strong regulation ability of ionic liquids.

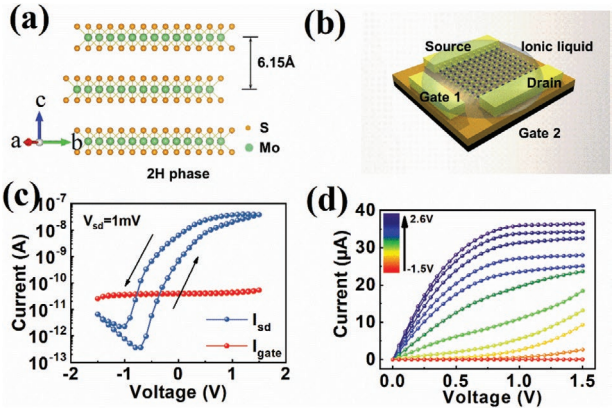

Figure 1. a) The crystal structure of 2H-MoS_2. b) The schematic illustration of the device structure. c) Transfer curve of the device. The source–drain current (I_{sd}) and the gate current (I_{gate}) were presented by the blue and red lines, respectively. The arrows denote the scanning direction during electrolyte gating. The applied V_{ds} is 1 mV in transfer curve. d) Output characteristics at different top gate biases.

2.2. Synaptic Plasticity Emulated by MoS_2 Transistors under Top Electrolyte Gating

The connection strength between presynaptic neurons and postsynaptic neurons is called the synaptic weight. Specific presynaptic action potentials can lead to a change in synaptic weight, which is considered to be the basis of learning and memorizing in the human brain. A typical excitatory post-synaptic current (EPSC) of the synaptic device triggered by the presynaptic spike (0.5 V, 5.5 ms) is shown in **Figure 2**a. Then, three presynaptic voltage pulses with different amplitudes (0.1, 0.5, 1.5 V) and a fixed pulse width of 5.5 ms were used to simulate the EPSCs of the synaptic device (Figure 2b). Short-term plasticity (STP) was transformed into long-term plasticity (LTP) with increasing the presynaptic pulse amplitude. Moreover, the transformation from STP to LTP could be realized by varying the pulse number and the pulse duration time (Figures S4 and S5, Supporting Information). Paired-pulse facilitation (PPF), as an important form of STP, which is involved in simple learning, information processing, sound source localization, and so on.[30,31] To emulate PPF, the top-gated MoS_2 transistor was triggered by top gate voltage pulses (0.5 V for 5.5 ms). The PPF can be obtained by the equations below.[32,33]

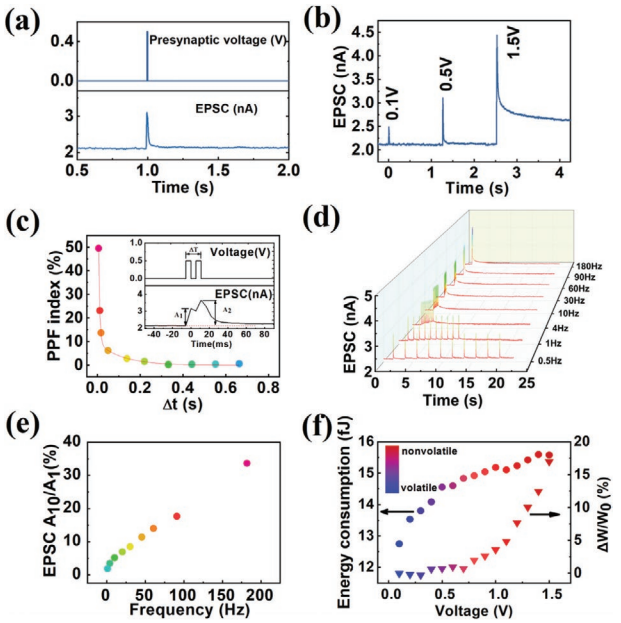

Figure 2. a) A typical EPSC of an MoS_2 synaptic device stimulated by a top gate voltage pulse (0.5 V, 5.5 ms). b) EPSC triggered by a series of presynaptic spikes, which are caused by top gate voltage with same duration time (5.5 ms) and different amplitudes (0.1, 0.5, and 1.5 V). c) The PPF index dependent time interval of two spatiotemporal correlated inputs. The double exponential decay function is used to fit the date of PPF index. Inset: pairs of presynaptic voltage pulses and the stimulated EPSC are plotted as a function of time. d) The EPSCs stimulated by a series of stimulus sequences with different frequencies varying from 0.5 to 180 Hz. e) Presynaptic spike frequency dependence of EPSC amplitude rate (A_{10}/A_1). f) The energy consumption per spike (left) and the long-term synaptic strength change (right) as a function of pulse amplitudes when the pulse width is fixed at 5.5 ms. ΔW is the synaptic strength change and W_0 is the initial synaptic strength for the artificial synapses.

$$\mathrm{PPF} = (\mathrm{A_2} - \mathrm{A_1})/\mathrm{A_1} \times 100\%$$

where A_1 and A_2 represent the first and second EPSC amplitudes, respectively. The PPF index dependent time interval of two spatiotemporal correlated inputs is shown in Figure 2c. A double exponential decay function fits the PPF index well,[34,35]

$$y = C_1 \exp\left(\frac{-t}{\tau_1}\right) + C_2 \exp\left(\frac{-t}{\tau_2}\right)$$

where t is the interval time of the presynaptic pulse, C_1 and C_2 are the initial facilitation magnitudes of the rapid and slow phases, and τ_1 and τ_2 are the characteristic relaxation times of the rapid and slow phases, respectively. All these parameters were extracted from the fitting equation: C_1 = 111.8%, C_2 = 9.7%, τ_1 = 5.39 ms, τ_2 = 111.87 ms for PPF. The distinction between τ_1 and τ_2 is clear, and the relaxation times are comparable to those in the biological synapse.[36] We further investigated the dependence of the EPSC on the pulse frequency (Figure 2d), and EPSC amplitude rate (A_{10}/A_1) was plotted as a function of the pulse frequency (Figure 2e). A good linear relation was obtained between the ratio and the frequency (Figure 2e). The ratio changed from 1.9% to 33.6%, as the frequency increased from 1 to 180 Hz. This behavior illustrates the potential application of our device in high pass filtering, which can be used to mimic sensory neural communication of the eye.[14] EPSC was stimulated by a series of presynaptic pulses voltage with the same duration time (5.5 ms) and different voltage amplitudes ranging from 0.1 to 1.5 V with a step of 0.1 V, as shown in Figure S6, Supporting information. The energy consumption can be calculated from the equation $E = I_P \times V_D \times t$, where I_P is the peak value (2.31 nA) of the EPSC, V_D is the applied drain voltage (1 mV), and t is the spike duration (5.5 ms). The energy consumption and corresponding long-term synaptic weight change were summarized as a function of presynaptic spike amplitude (Figure 2f). It should be noted that when the presynaptic spike amplitude was as low as 0.1 V, the minimum value of the energy consumption per spike in the short-term mode was obtained at 12.7 fJ.

It can be seen that the long-term weight change was increased with increasing the voltage amplitudes. Spike timing-dependent plasticity (STDP) is a biological process that regulates the strength of neuronal connections and exhibits temporal asymmetry. To mimic STDP in the device, we used a multiplexer to convert the pre- and post-neuron spikes, and the output terminal was connected to the top gate electrode (Figure S7c, Supporting Information). The waveform of the preneuron spikes and postneuron spikes was shown in Figure S7a,b, Supporting information. A typical asymmetric form of STDP was demonstrated in our electrolyte-gated synaptic transistor (Figure S7d, Supporting Information).

2.3. Simulation of Image Classification

In synaptic transistors, the change of channel conductance leads to the change of synaptic weight. We realized long-term potentiation and depression processes by changing the channel conductance. The long-term potentiation process was driven by 20 top gate voltage pulses (1 V for 6 ms spaced 1 s apart), while the long-term depression process was driven by 20 top gate voltage pulses (–0.9 V for 6 ms spaced 1 s apart). The conductance of the channel was varied from 1.8 to 3.8 μS. The potentiation and depression processes can be mimicked continuously by applying consecutive positive and negative spikes, reflecting reproducible switching (**Figure 3**a). We simulated the performance of an artificial neural network using the experimentally measured conductance states (Figure 3a) for training with back-propagation of two data sets, a small image version (8 × 8 pixels) of handwritten digits from the "Optical Recognition of Handwritten Digits " dataset,[37] and a large image version (28 × 28 pixels) of handwritten digits from the "Modified National Institute of Standards and Technology" dataset.[38] A three-layer artificial neural network with one hidden layer was utilized in our simulations using CrossSim simulator (Figure 3b). The hardware implementation with the synaptic layer is given in a schematic illustration (Figure 3c). By comparing with the performance of the ideal floating-point-based neural network, the evolution of recognition accuracy with training epochs for small and large digits is plotted in Figures 3d and 3e, respectively. For the small digits, the recognition accuracy approached 90% within the second training epoch, and the recognition accuracy remained 94.5% after 17 training epochs. In contrast, the maximum of

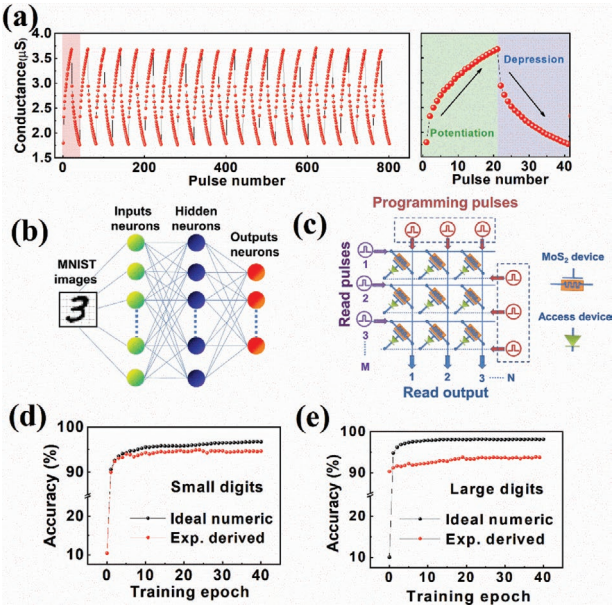

Figure 3. a) Channel conductance variation versus pulse number (left). Twenty distinct states are shown for the long-term potentiation and depression processes, respectively, which are triggered by repeated positive and negative top gate voltage pulses. The zoom-in view (right) shows the first cycle. b) Schematic image of a three-layer neural network. c) Schematic image of the synaptic layer made up of electrolyte-gated MoS_2 transistor crossbar array and access device. Evolution of recognition accuracy with training epochs for d) small and e) large digits.

the ideal floating-point-based neural network was estimated to be 96.7%. For the large digits, compared to the maximum of 98.2% for the ideal floating-point-based neural network, the recognition accuracy could exceed 90% within the second training epoch, and reached 93.9% after 40 training epochs. The recognition accuracy of the MoS_2 based synaptic transistor for the large digits is slightly lower than that obtained by others in recent experiments.[39,40] However, the present result is higher than the two-terminal resistive memory devices.[41,42] To improve the device performance, there is still a lot of work to be done to improve the linearity and symmetry in the process of the rising and falling conductance variation process, which is key to improve the recognition accuracy.[40]

2.4. Dynamic Process of Short and Long-Term Memories

To concretely mimic the short- and long-term memories, images "C," "A," and "S" were written alternately on a 5 × 7 synapse array, by applying 30 voltage pulses with top gate voltages at 0.4, 1.5, and 0.4 V, respectively (**Figure 4**). The 35 synapse array was operated on individual devices. The duration and time interval were fixed at 6 ms for each training sequence. The initial state of the synaptic array was shown in Figure 4a, where the color level and the height exhibited the values of conductance in the whole process. Then, the image of "C" was imported into the synapses array by applying a series of top gate voltage pulses (0.4 V for 6 ms with an interval of 6 ms, 30 pulses) (Figure 4b). After 4 s, the image of "C" could not be distinguished (Figure 4c), which indicates the short-term memory behavior of this process. Next, by applying repeated top gate voltage pulses (1.5 V for 6 ms with an interval of 6 ms, 30 pulses), the image of "A" was imported into the synapse array (Figure 4d). The image of "A" could be maintained after period 4 s, which demonstrates long-term memory (Figure 4e). Then, the image of "S" was inputted by using low top gate voltage pulses (0.4 V for 6 ms with an interval of 6 ms, 30 pulses) (Figure 4f). After 4 s, the image of "S" disappeared while the image of "A" could still be recognized (Figure 4g), which demonstrates the difference between short- and long-term memories. In the end, the image of "A" was erased from the synapses array by using

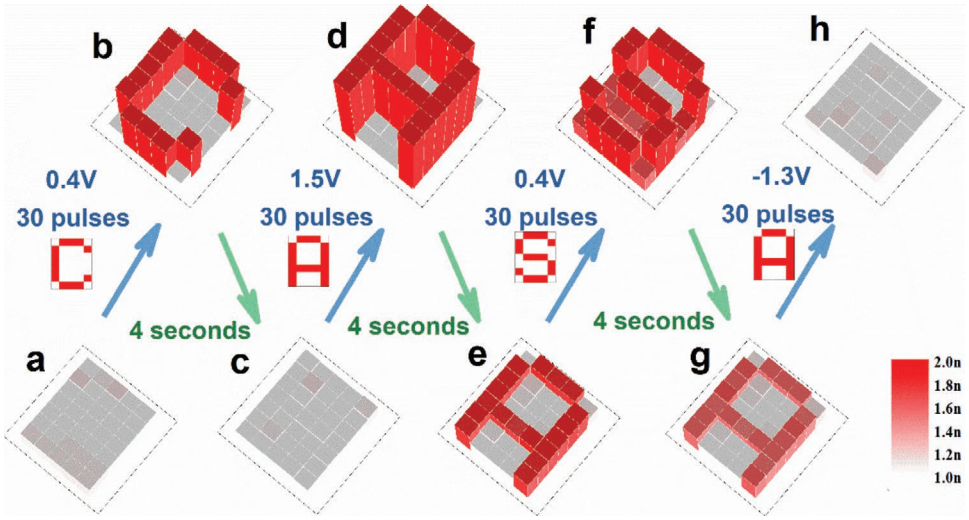

Figure 4. Dynamic process of STM and LTM in a synaptic array. a) The initial state of the synaptic array. b) The image of "C" was inputted into the synapse array by applying a series of top gate voltage pulses (0.4 V for 6 ms with an interval of 6 ms). c) After a period (4 s), the image of "C" could not be distinguished. d) The image of "A" was imported into the synapses array by using repeated top gate voltage pulses (1.5 V for 6 ms with an interval of 6 ms). e) The image of "A" could be recognized in 4 s. f) The image of "S" was inputted by using the same voltage series as stage (b). g) The image of "A" could be recognized while the image of "S" disappeared. h) The image of "A" was erased from the synapses array by using a reverse top gate voltage.

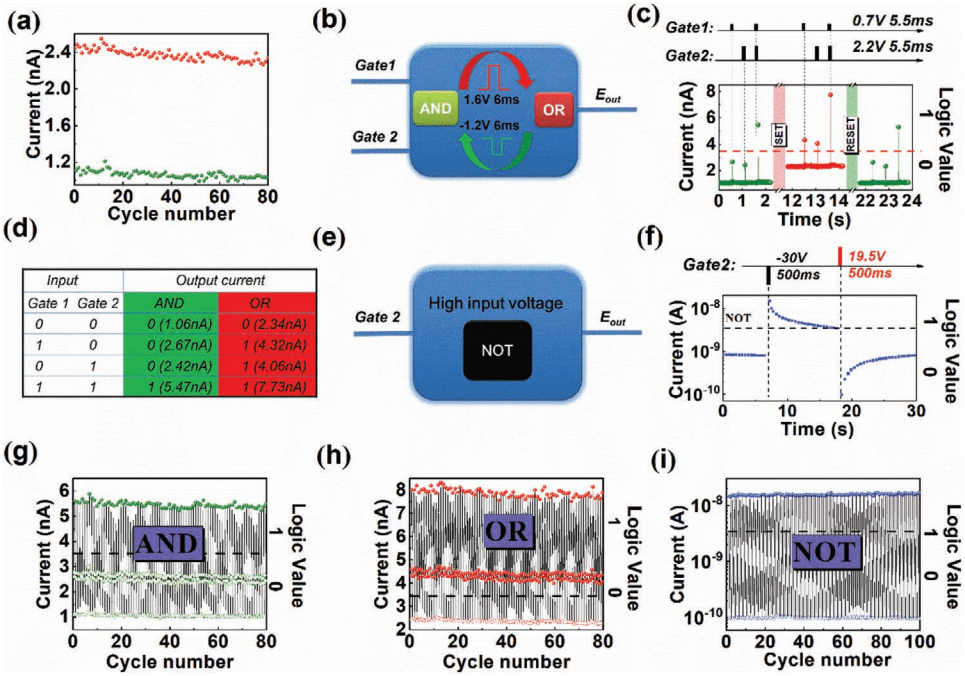

Figure 5. a) Modulation between the high and low resistance states. b) A schematic illustration of the logical converter between the "AND" logical operation and "OR" logical operation. c) Dynamic reconfiguration of logic operation: two different logic responses were drawn by the red and green lines. Two stimulus pulses, 0.7 V for 5.5 ms and 2.2 V for 5.5 ms, were applied to the Gate 1 and Gate 2 respectively. Set process: a presynaptic spike (1.6 V for 6 ms) is applied on the Gate 1 for transfer the "AND" logical operation to the "OR" logical operation. Reset process: a presynaptic spike (–1.2 V for 6 ms) is applied on the Gate 1 for transfer the "OR" logical operation to the "AND" logical operation. d) The truth table and output current for different logical operations. e) Schematic illustration of the "NOT" logical operation. f) The dynamic process of the "NOT" logical operation: two stimulus pulses, –30 V for 500 ms and 19.5 V for 500 ms, were applied to the Gate 2. Endurance property of g) "AND," h) "OR," and i) "NOT" operations.

a reverse top gate voltage (Figure 4h). The typical EPSC curve corresponds to one of the pixel was shown in Figure S8, Supporting Information. In summary, the experiment successfully demonstrated the coexistence of the short- and long-term memories in the proposed artificial synapse.

2.5. Configurable Logic Operations with Dual Gating

The decision-making ability in human brain is owed to the different logic operations.[43] Programmable logic circuits, which can dynamically reconfigure the logic operations, are considered as an effective approach to enhance these functions.[26,27,44,45] Here, we demonstrated that the dual gated MoS_2 transistor can dynamically reconfigure the logic operation. As shown in Figure 1b, the top electrolyte gate (Gate 1) and the back gate (Gate 2) were regarded as two input terminals, while the drain was regarded as the output terminal. The source electrode was always grounded. When a voltage pulse (1.6 V for 6 ms) was applied to Gate 1, the transistor changed to a more conductive state. On the contrary, a voltage pulse (–1.2 V for 6 ms) was applied to Gate 1 to recover its pristine state. The conductance states can be switched reversibly (**Figure 5**a). A schematic illustration of the logic operations was shown in Figure 5b. A voltage pulse (1.6 V for 6 ms) was applied to the Gate 1 to convert "AND" logic into "OR" logic, and then a voltage pulse (–1.2 V for 6 ms) was applied to reverse the logic back. Here, a threshold current (3.5 nA) was set for the postsynaptic current to define the "0" and "1" states. Figure 5c showed the dynamic process of logical operation and logical transformation. The red dotted line represented the threshold current. At the initial low conductance state, the output current could exceed the threshold when both inputs occurred simultaneously ("AND" logic). When the device reached its high conductance state, as long as one of the two inputs occurred, the output current could exceed the threshold ("OR" logic). The truth table summarizes both types of logic (Figure 5d) in which the postsynaptic current was obtained from Figure 5c. When the input voltage was high for Gate 2, the induced postsynaptic current was opposite to the polarity of the input voltage due to the electron trapping.[14] The output level was opposite to the input level. This characteristic could be utilized to simulate "NOT" logic and the schematic illustration was shown in Figure 5e. The dynamic process of the "NOT" logical operation was shown in Figure 5f. The dotted line represented the threshold current (3.5 nA).

To investigate the endurance property of the logic operation and switching, we repeated the process of "AND logic-set-OR logic-reset," and the cyclic results of "AND" logic and "OR" logic was shown in Figures 5g and 5h, respectively. Hollow spheres represented the postsynaptic spike current below the threshold (dotted line), that is, the "0" state, while the solid sphere represents the postsynaptic spike current above the threshold (dotted line), that is, the "1" state. It should be noted that the postsynaptic spike currents triggered by Gate 1 were almost equal to the one triggered by Gate 2, and thus they are

Table 1. Device performance in 2D material transistors.

Materials	External electrolyte	Nonvolatile logic operation	Neuromorphic computing	Refs.
WSe_2	Li^+	No	No	[13]
MoS_2	DEME-TFSI	No	No	[14]
MoS_2	Li^+	No	Yes	[46]
MoS_2	Chitosan	No	No	[25]
MoS_2	PVA	No	No	[23]
MoS_2	PVA	No	No	[21]
MoS_2	PVA	No	No	[24]
MoS_2	DEME-TFSI	Yes	Yes	This work

indistinguishable. The endurance property of the "NOT" logic was also investigated (Figure 5i), indicating good device performance. Thus, We realized both synaptic and programmable logic operation functions in this dual-gated MoS_2 transistor, different from other works (**Table 1**).

2.6. Simulation of Pavlov's Dog Experiment

Pavlov's dog experiment, a classical conditioning experiment, is one of the expression forms of the associative learning in the brain, that is, creating the association between the presynaptic inputs. Here, the proposed device was used to simulate this experiment (**Figure 6**). First, the EPSC (1.75 nA) was defined as the threshold current for the dog's salivation response drawn by a red dotted line. Here, the voltage pulses applied to Gate 1 were used to simulate the unconditioned stimuli (feeding the bone) causing the unconditioned response (salivation), that is, the EPSC exceeded the threshold current (Stage (i)). The voltage pulses applied to Gate 2 were used to simulate the conditioned stimuli (ring the bell) as shown in Stage (ii) Initially, an effective association between unconditioned stimuli (feeding the bone) and conditioned stimuli (ring the bell) was not built by a short period of training (5.5 ms) with simultaneous feeding and ringing the bell (Stage (iii)). However, when the training time increased to 10 s, the association between unconditioned stimuli and conditioned stimuli was strengthened, after which the dog's salivation could be caused by conditioned stimuli alone (Stage (iv)). Nevertheless, without the repeated training with simultaneous unconditioned and conditioned stimuli, the efficient conditioned response weakened and disappeared gradually (Stage (v)). It is similar to forgetting of old information in the brain, which is considered to be essential to the efficient functioning of the mind. Finally, as shown in Stage (vi), the association could get back to previous levels after a shorter time training (5 s), similar to the biological learning curve, due to the electron accumulation induced by repeated training. It should be noted that the built association could be removed

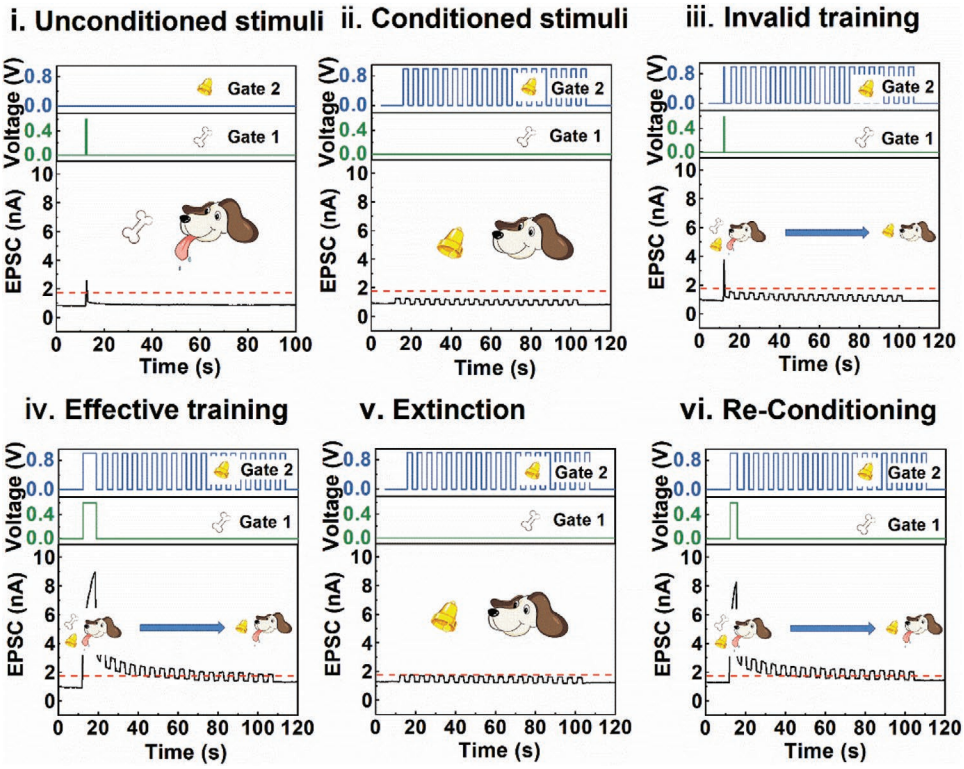

Figure 6. Schematic diagram of the outline of Pavlov's dog experiment. i) Unconditioned stimuli. ii) Conditioned stimuli. iii) Initial training with simultaneous application of unconditioned and conditioned stimuli did not result in effective association. iv) With an increase in the training sequences, the association between unconditioned and conditioned stimuli was strengthened, after which the conditioned stimuli could produce salivation, indicating efficient response. v) However, without repeated training with simultaneous unconditioned and conditioned stimuli, the efficient conditioned response weakened and disappeared gradually. vi) The same level of association was rebuilt after a short-time training.

rapidly when the specific stimuli (–1.2 V, 5.5 ms) was applied to Gate 1 (Figure S9, Supporting Information). This reflected that an aversive stimulation could result in the damage of the efficient association to emulate the destruction of conditioned responses by other stimuli.

3. Conclusion

In summary, the dual gated synaptic transistor based on the MoS_2 flake with a thickness of 5.6 nm was fabricated. The device exhibited large on/off ratio ($I_{on}/I_{off} > 10^5$) in the transfer curve, and good pinch-off characteristics in the output curves. The device under top electrolyte gating successfully emulated synaptic plasticity and STDP. Furthermore, it exhibited ultra-low energy consumption (12.7 fJ), which can be comparable to the biological synapses. By combining top electrolyte gating and back gating together, the MoS_2 based synaptic transistor realized configurable logic operations of "AND," "OR," and "NOT," and simulated Pavlov's dog experiment. All the results indicated that the dual gated MoS_2 synaptic transistor has a potential application in neuromorphic and programmable logic devices.

4. Experimental Section

Device Fabrication: The 2H-MoS_2 sheet was exfoliated from bulk crystal and transferred onto an n-type silicon substrate with a 300 nm thick SiO_2 surface layer. Electron-beam lithography was used to define patterns for metal contacts on PMMA resist spin coated over the flakes and the Au electrodes were deposited using the thermal evaporation technique. The ionic liquid DEME-TFSI was utilized as a dielectric layer, covering the MoS_2 channel and the top gate electrode.

Characterization Measurements: The Raman characterization was obtained by using the alpha300 R microscope under 532 nm laser excitation. By using an optical microscope, the thin flake was identified, and then the flake thickness was defined by an AFM.

Electrical Measurements: All the electrical measurements were conducted in a Lakeshore probe station using Keithley 4200 semiconductor parameter analyzer at the ambient conditions. The source–drain current I_{sd} was measured using 4200 SMU module with preamplifier, while the gate leakage current I_{gate} was measured using 4200 SMU module. During the measurements, a constant voltage 2 mV was applied to the source–drain electrodes to read the current for the configurable logic operations, and 1 mV was applied to the source–drain electrodes for other measurements. The scanning rate is 5 mV s^{-1} during measuring the transfer curve.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

logic operations, MoS_2, neuromorphic computing, synaptic transistors

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