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A Ferrite Synaptic Transistor with Topotactic Transformation

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Hardware implementation of artificial synaptic devices that emulate the functions of biological synapses is inspired by the biological neuromorphic system and has drawn considerable interest. Here, a three-terminal ferrite synaptic device based on a topotactic phase transition between crystalline phases is presented. The electrolyte-gating-controlled topotactic phase transformation between brownmillerite $SrFeO_{2.5}$ and perovskite $SrFeO_{3-\delta}$ is confirmed from the examination of the crystal and electronic structure. A synaptic transistor with electrolyte-gated ferrite films by harnessing gate-controllable multilevel conduction states, which originate from many distinct oxygen-deficient perovskite structures of $SrFeO_x$ induced by topotactic phase transformation, is successfully constructed. This three-terminal artificial synapse can mimic important synaptic functions, such as synaptic plasticity and spike-timing-dependent plasticity. Simulations of a neural network consisting of ferrite synaptic transistors indicate that the system offers high classification accuracy. These results provide insight into the potential application of advanced topotactic phase transformation materials for designing artificial synapses with high performance.

Learning and memory in the human brain occur through dynamic changes in the connection strength between interconnected networks of biological synapses.[1] The human brain can process data and identify patterns more robustly than any computer, primarily due to this synaptic connection between neurons.[2] Thus, designing artificial synapses with the functionality of biological synapses is essential for hardware implementation of neural networks that emulate synaptic functions.[3] Synaptic plasticity and nonvolatility are the key features that mimic learning and memory in a synapse.[4] Silicon-based complementary metal-oxide-semiconductor (CMOS) circuits using tens of transistors were used to mimic synaptic activity.[5] However, this approach requires a very large area and consumes a significant amount of power, hindering its further development.[6] Two-terminal memristors based on metal oxides,[7–12] ferroelectric,[13,14] and phase-change materials[15,16] have attracted much attention as nonvolatile memory that can emulate synaptic functions, such as synaptic plasticity and spike-timing-dependent plasticity (STDP). A variety of tunable resistance states in these devices were utilized to store the synaptic weight, exhibiting synaptic plasticity.[17] More recently, three-terminal electrolyte-gated transistors were proposed for application as artificial synapses. With an additional gate control, three-terminal devices seem to be favorable for realizing synaptic functions[18–22] with low energy consumption.[4,23,24] The signal transmission and learning processes can be performed concurrently because the signal transmission is carried through the channel and the synaptic weight is manipulated via the gate terminal.[17] Such synaptic transistors greatly enrich neuromorphic devices, which provide a promising method for creating artificial neural networks.[25,26] This requires advanced thin film materials for fabricating the channel, in which it should have multilevel resistance states under electrolyte gating.

Topotactic phase transitions in functional oxides enable reversible structural changes between crystalline phases. This is different from a phase change between amorphous and crystalline states, which is the foundation of phase-change memory.[27] A topotactic phase transition provides an effective method for manipulating physical properties by modulating oxygen stoichiometry within functional oxides.[28,29] Strontium ferrite $SrFeO_x$ (SFO) with topotactic phase transformation has been recently investigated in many technological applications such as fuel cells, oxygen sensors, resistive memories, and catalysts.[30–33] The crystal structure of SFO exhibits a variety of distinct oxygen-deficient perovskite (PV) structures with x ranging from 2.5 to 3, depending on its oxygen stoichiometry.[29,34–36] Brownmillerite (BM)-SFO with the alternating layers of FeO_6 octahedra and FeO_4 tetrahedra (**Figure 1**a) is an insulator, while PV-SFO with corner-sharing FeO_6 octahedra (Figure 1b) exhibits metallic conduction due to vacancy filling with oxygen atoms.[32,35,36] Most of works realized topotactic phase transition of SFO by controlling redox reactions under various oxygen atmosphere conditions, hindering its application in neuromorphic electronic devices. In recent years, ionic liquid gating (ILG) has emerged as an intriguing method for manipulating

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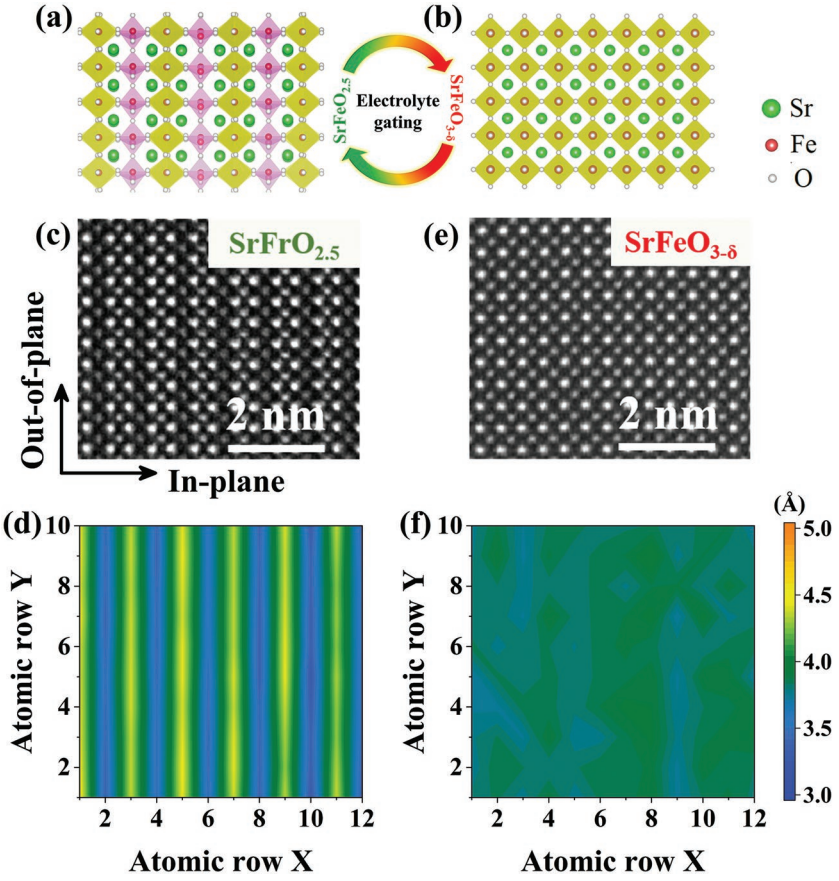

Figure 1. Evolution of the structural phase via electrolyte gating. a,b) The schematic crystal structures of brownmillerite $SrFeO_{2.5}$ (a)and perovskite $SrFeO_{3-\delta}$ (b) thin films along the [100] direction in the $SrTiO_3$ substrate are presented. c,d) Cross-sectional HAADF-STEM image (c) and in-plane Sr–Sr distance (d) in the pristine BM $SrFeO_{2.5}$ films. e,f) Cross-sectional HAADF-STEM image (e) and in-plane Sr–Sr distance (f) in the gated PV $SrFeO_{3-\delta}$ films.

material properties, not only via an electrostatic effect,[37] but also via an ion-migration-induced phase transformation, which is an electrochemical effect.[38,39] The pioneering work performed by Lu et al. shows that reversible phase transformations among different phases can be achieved through ILG-controlled insertion and extraction of functional ions in cobaltite films.[38] This result shows that a topotactic phase-change material may be a good candidate for fabricating the channel in electrolyte-gated synaptic transistors.

In this work, we report a reversible topotactic phase transformation in $SrFeO_x$ ($2.5 \le x \le 3.0$) epitaxial thin films through electrolyte gating. We constructed a synaptic transistor with ionic-liquid-gated SFO films by exploiting the continuous topotactic phase change. This synaptic transistor exhibits important synaptic functions, including potentiation, depression, and STDP. The synaptic transistors with topotactic phase transitions between BM and PV phases in SFO thin films proposed here open a new approach for building future neuromorphic systems.

BM-SFO epitaxial thin films were grown on a (001)-oriented $SrTiO_3$ (STO) substrate using pulsed laser deposition (see the Experimental Section for details). X-ray diffraction (XRD) and X-ray reciprocal-space mapping (RSM) patterns imply that the as-grown film contains an out-of-plane BM phase, whose oxygen-deficient FeO_4 tetrahedral layers are perpendicular to the film surface (Figure S1a,b, Supporting Information).[34,36,40] We subsequently investigate the structural transformation between BM and PV phases through ILG. As-received ionic liquid *N,N*-diethyl-*N*-(2-methoxyethyl)-*N*-methylammonium bis-(trifluoromethylsulphonyl)-imide (DEME-TFSI) was used as the electrolyte gating medium. Thanks to the nonvolatile feature of topotactic phase transition, we can perform various ex situ measurements to explore changes in the SFO films after gating. After ILG, the crystal structure of the thin film transformed into a PV-like structure (Figure S1c,d, Supporting Information). We monitored in situ XRD θ–2θ scans of the SFO epitaxial film during ILG in order to directly observe the structural phase transformation (Figures S2, Supporting Information). These structural measurements imply that ILG-induced transformations between BM and PV phases are controllable and nonvolatile. The oxygen required during the topotactic phase transformation could come from the atmosphere[41] and the water content of ionic liquid.[38,39] Scanning transmission electron microscopy (STEM) results further confirm that the phase transformation between BM and PV in SFO films occurs via ILG at the atomic scale. Alternating stacking of oxygen-deficient tetrahedral (FeO_4) and fully oxygenated octahedral (FeO_6) sublayers is manifested by the periodic dark stripes in a high-angle annular dark field (HAADF) STEM image (Figure 1c). The in-plane Sr–Sr atomic distances in the tetrahedral and octahedral sublayers are about 4.4 and 3.4 Å, respectively (Figure 1d). A typical PV structure was clearly observed in the SFO films after negative gating (Figure 1e). The in-plane Sr–Sr atomic distance is about 3.83 Å (Figure 1f). The in-plane and out-of-plane lattice constants obtained from HAADF-STEM images are summarized in Figure S3 in the Supporting Information.

The associated electron energy loss spectra (EELS) (Figure S4, Supporting Information) and X-ray absorption spectroscopy (XAS) (Figure S5, Supporting Information) also reveal a phase transformation from BM to PV phases after negative gating. The pristine BM-SFO thin film is insulating, while the PV-SFO thin film formed via ILG is more conductive (Figure S6, Supporting Information). Moreover, we could electrically switch the film color with bias gating, and the color changes from light yellow to opaque (Figure S7, Supporting Information). All these physical features make electrolyte-gated SFO thin films highly intriguing for potential applications in robust synaptic transistors.

We designed an electrolyte-gated transistor architecture using pristine BM-SFO epitaxial films as the channel material

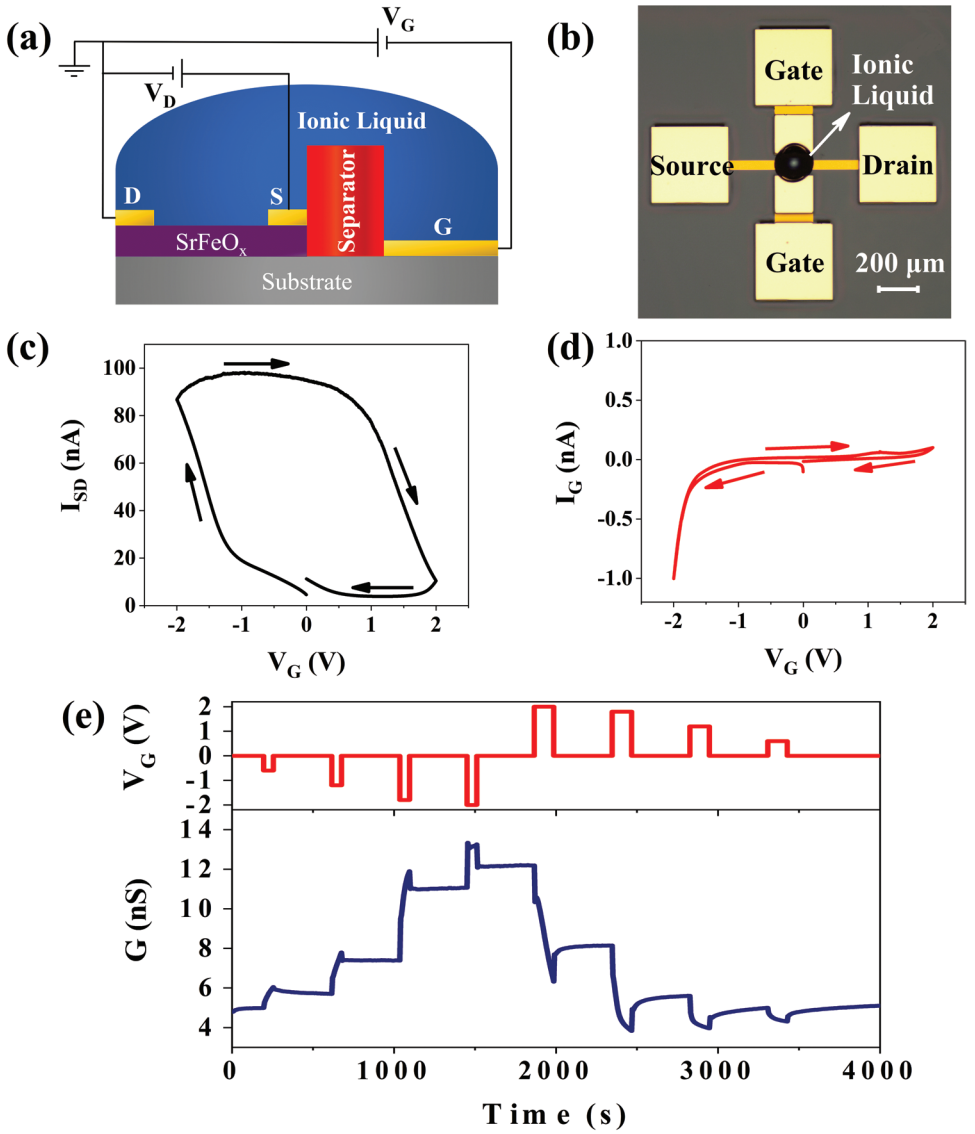

Figure 2. Electrolyte-gated ferrite transistor. a) The schematic illustration of the transistor structure and measurement setup. $SrFeO_x$ films form the channel between source (S) and drain (D) electrodes, and an ionic liquid (DEME-TFSI) is used as the gating medium. b) An optical image of a typical ferrite transistor device showing a droplet of the ionic liquid. c) Sheet conductance versus gate bias. Here, the gate voltage V_G was swept at 1 mV s^{-1}. Arrows show the direction of the gate bias sweep. d) Gate leakage current during the transfer curve measurement. e) Sheet conductance G versus time for 65 s pulses spaced 6 min apart in the negative gate sequence −0.6, −1.2, −1.8, and −2.0 V, and 125 s pulses spaced 6 min apart in the positive gate sequence 2.0, 1.8, 1.2, and 0.6 V. The source–drain voltage V_{SD} = 0.6 V.

in order to emulate the functions of biological synapses. **Figure 2**a shows a schematic illustration of the device structure. The as-grown BM-SFO films were patterned to microscale channels with coplanar gate electrodes using standard optical lithographic techniques (see the Experimental Section for details). Figure 2b shows an optical image of a typical device with a droplet of the DEME-TFSI IL. The gate voltage V_G was swept at 1 mV s^{-1}, and the source–drain voltage V_{SD} 0.6 V. The transfer curve shows a clear hysteresis loop, indicating good reversibility (Figure 2c).[41] The gate leakage current I_G is about two orders of magnitude smaller than the source–drain current I_{SD}, reflecting I_G has a negligible effect on device performance (Figure 2d). The channel could be reversibly manipulated between low and high conductance states. The device conductance increases as V_G is swept from 0 to negative values, while the device conductance decreases when $V_G > 0$. The transfer curve is consistent with the occurrence of a topotactic phase transition of SFO films. Negative gating can trigger the transformation from the insulating BM phase to the conductive PV phase in the SFO films, while positive gating can induce the transformation from the conductive PV phase back to the insulating BM phase in the SFO films.

To demonstrate the multilevel states required for synaptic functions, the electrolyte-gated SFO transistor was operated by sending a series of voltage trains to the gate electrode (Figure 2e). The voltage trains consist of a "write" operation,

where a series of V_G pulses are sent to the gate electrode. During the voltage trains, there is always "read" operation, where the channel conduction is measured with V_{SD} = 0.6 V. The conductance (≈5 nS) of the SFO-based synaptic transistor is very low, compared with that of most of synaptic transistors (Table S1, Supporting Information). Ultralow conductance is particularly important for designing neural networks with large-scale device arrays. Initially, the BM-SFO channel conduction was kept constant at zero bias for 200 s, and thus the chemical reaction could be excluded when V_G = 0. Here, a negative voltage train causes a stepped increase in the channel conduction from 5 to 12 nS. During each negative "write" operation, the conduction increases due to the phase transformation in the SFO channel from insulating BM to conductive PV. A higher V_G value can induce larger channel conduction modulation. The channel conduction can remain constant after each "write" operation, implying intrinsic nonvolatile behavior. The nonvolatility originating from the structural phase stability is essential for realizing neuromorphic devices that consume low energy. These voltage-controlled multilevel states form based on mixed phases of insulating BM and metallic PV in various proportions. The channel conduction can be increased by applying a negative V_G, but it can also be decreased by applying a positive V_G (Figure 2e). The induced state could keep stable for at least 2×10^4 s, demonstrating good retention property (Figure S8, Supporting Information). It is worth mentioning that the induced PV-SFO films via topotactic phase transformation are still stable after one year. Good retention is particularly important for an artificial neural network that is trained offline. A subsequent train of positive V_G pulses returns the device conductance to its initial state. The electrolyte-gated ferrite transistor with V_G-controlled multilevel conduction states provides a unique opportunity to design synaptic devices.

Taking advantage of the voltage-controlled multilevel conduction states, we show that the electrolyte-gated ferrite transistor displays the synaptic functions that are the building blocks of neuromorphic devices. The triggering of excitatory postsynaptic current (EPSC) is a key feature that underlies the main process of neuronal transmission. In order to evaluate the synaptic responses in the SFO transistor, we applied a series of presynaptic spikes with different bias amplitudes to the gate electrode, and we simultaneously monitored the source–drain current (I_{SD}) with V_{SD} = 0.6 V. The pulse width was fixed at 5 s. Obviously, the presynaptic spike (V_G) triggered a postsynaptic current (I_{SD}) in the SFO channel (**Figure 3**a). The EPSC can be varied by changing the amplitude of the V_G pulses. The transition from short-term memory to long-term memory exploits electrostatic and electrochemical effects and occurs as V_G increases (Figure 3a).[24] Here, we primarily focus on mimicking the long-term phenomena of biological synapses by harnessing the topotactic phase transition in SFO films. Furthermore, EPSC could be modulated by varying the pulse width of the presynaptic spikes. The amplitude of the applied gate pulse was fixed at −2 V. The peak and retention EPSC values triggered by the gate pulse increase as the pulse width increases (Figure 3b). Figure 3c shows that bistable conduction states can be controlled by sending alternating negative and positive gating pulse to the electrolyte-gated SFO transistor. 16 negative V_G pulses with −1.8 V amplitude were applied to increase the conduction from 4.8 to 7.8 nS. Then, 24 V_G pulses with +1.8 V amplitude and pulse width of 10 s pulse width were used to switch the conduction state. The conduction gradually decreased from 7.8 to 4.8 nS. Repetitive cycles of these measurements show that the nonvolatile memory behavior is exactly reproducible, where the V_G procedure during the first cycle was repeated.

The essential synaptic attribute that should be mimicked in synaptic devices is synaptic plasticity, which is the ability of the synapse to change its weight.[42] Long-term plasticity, which commonly exists in biological synapses, consists of long-term potentiation (LTP) and long-term depression (LTD),[43] respectively defined as a persistent increase and a persistent decrease in the synaptic weight. These states can be reached by applying a number of consecutive gate pulses to tune the device's conductance via a topotactic phase transformation. LTP is widely regarded as the important foundation that underlies learning and memory in biological systems.[44] Figure 3d shows the dependence of LTP as a function of the number of pulse, where the pulse amplitude and width are fixed at −1.8 V and 5 s, respectively. Because an increased number of negative gate pulses will effectively increase oxygen intercalation in the SFO channel, one can find that the channel conduction will monotonically increase during the gradual transformation from the insulating BM-SFO phase to the conductive PV-SFO phase. Such behavior effectively emulates LTP in biological synapses. In contrast, LTD is utilized to selectively weaken synapses and hinder further encoding of new information after LTP. LTD occurs when positive synaptic spikes were applied to the gate electrode. To demonstrate LTD, we applied 24 consecutive gate spikes in the synaptic transistor, with an amplitude of +1.8 V, a pulse width of 10 s, and an interval of 10 s (Figure 3d). Positive gating tends to extract oxygen ions from the SFO channel, causing a transformation from the metallic PV phase to the insulating BM phase. Therefore, successive positive gate spikes will decrease EPSC. The potentiation and depression of synaptic weight can be mimicked continuously by applying consecutive negative and positive spikes, reflecting reproducible and nonvolatile switching (Figure 3d). It should be noted that we here applied wide gate pulses in order to make the conduction modulation obvious during a single operation. LTP and LTD processes can also be realized by using narrow gate pulses (Figure S9, Supporting Information). The energy consumption per spike (≈4.8 pJ) is orders of magnitude lower than that (≈900 pJ) of artificial synapses based on conventional CMOS circuits.[5] It can be comparable to that of the reported electrolyte-gated synaptic transistors, and higher than several recent memristive reports (Table S1, Supporting Information). The present results imply that the SFO device can potentially simulate the synaptic plasticity that occurs in biological synapses.

STDP, which is considered to be one of the essential Hebbian learning rules for emulating synaptic functions, refers to a change in the synaptic weight as a result of correlated pre- and postneuron spikes based on synaptic plasticity.[45–47] Synaptic weight modulation strongly depends on the time difference Δt between the pre- and postneuron spikes, facilitating precise control over sign and magnitude of the synaptic weight change. Based on the plasticity of the channel conductance in the electrolyte-gated SFO transistor, we successfully

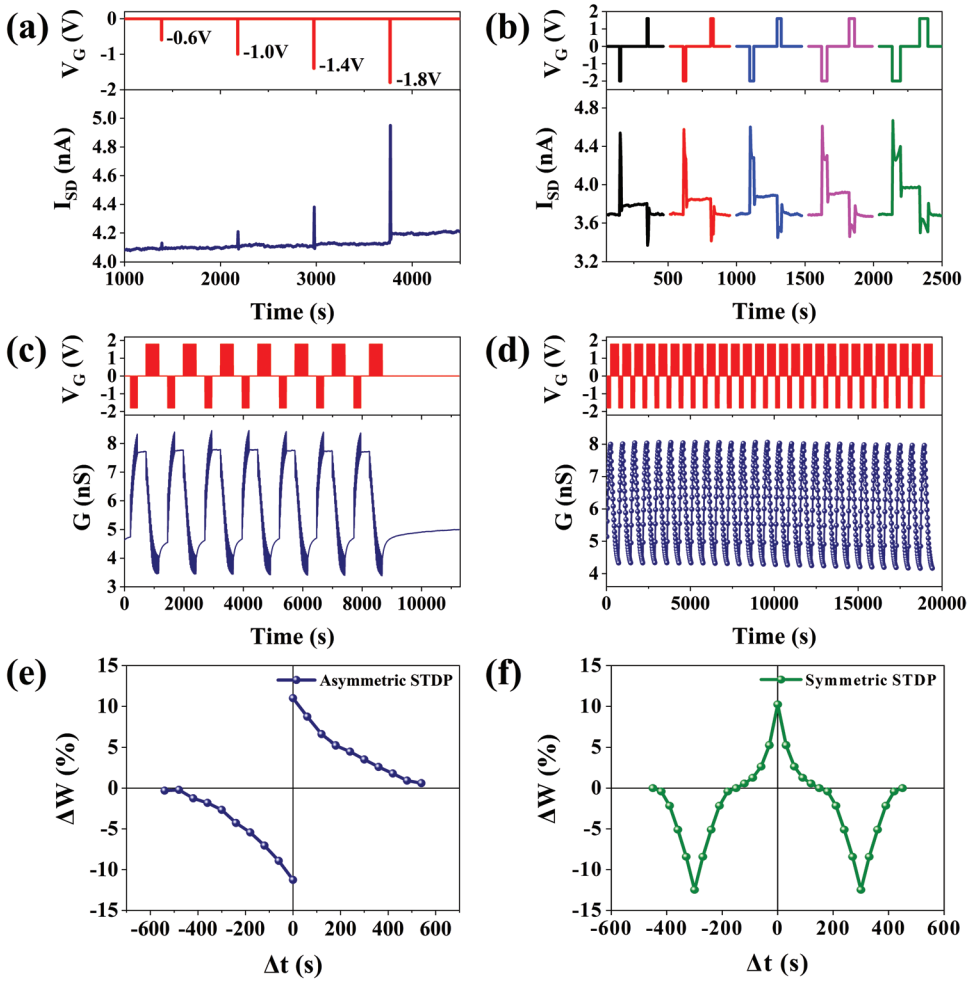

Figure 3. The characteristics of ferrite synaptic transistor for neuromorphic computing. a) EPSC induced by a series of gate voltage pulses with the same pulse width (5 s) and different amplitudes (–0.6, –1.0, –1.4, and –1.8 V). b) EPSC induced by a series of gate voltage pulses with the same amplitude (–2.0 V) and different pulse widths (10, 20, 30, 40, and 60 s). c) Sheet conductance modulation versus time by applying two gate voltage pulses (–1.8 and 1.8 V) and retention property at zero bias. 16 and 24 pulses were used at –1.8 and 1.8 V, respectively. The pulse width is 5 s and the interval is 10 s. d) V_G-controlled long-term potentiation and depression behavior with 16 negative (–1.8 V for 5 s, spaced 10 s apart) and 24 positive (1.8 V for 10 s, spaced 10 s apart) V_G pulses. e,f) Asymmetric (e) and symmetric (f) STDP functions implemented in the ferrite synaptic transistor. Here, Δt is the difference between the pre- and postneuron spikes.

show that the proposed transistor exhibits an STDP function. In order to mimic the STDP function, the output terminal of a multiplexer was connected to the gate electrode of the transistor and was used to convert the time difference between pre- and postneuron spikes to a voltage pulse.[25,48] More details regarding this circuitry can be found in Figure S10 in the Supporting Information. The percentage change in the channel conductance in an SFO transistor with a series of Δt from –600 to 600 s suggests a typical asymmetric STDP function (Figure 3e). Regarding asymmetric STDP, LTP will occur if the preneuron spike arrives prior to the postneuron spike ($\Delta t > 0$), while LTD will occur if the preneuron spike arrives after the postneuron spike ($\Delta t < 0$). The obtained asymmetric STDP curve can be fitted to an exponential decay function and mimics the behavior of a biological synaptic system.[45] The symmetric STDP function can also be realized by choosing the appropriate shape of the source spike (Figure 3f). For the symmetric STDP, the change in the channel conductance only depends on the absolute value of Δt. The successful implementation of STDP in a ferrite-based transistor indicates the introduction of an advanced material system for developing neuromorphic devices.

In order to concretely mimic potentiation and depression during electrical stimulation, images "I," "O," and "P" were written and erased from a 3 × 5 synapse array (**Figure 4**). Fresh artificial synapses with low conductance were arranged in an array format. Then, the image of the letter "I" was written into the synapse array using 28 pulses with a –1.8 V gate amplitude (Figure 4a). The duration and interval between gate pulses were 2 and 4 s, respectively. The channel conductance is increased from 5 to 6.7 nS while the pulse train was applied. An image of the letter "I" was successfully stored in the synapse array, and the image can persist during one hour due to the topotactic phase transition. This nonvolatile process shows how these artificial synapses can be used to store data. The fault tolerance was tested by applying spurious pulses (–0.3 V amplitude, 2 s

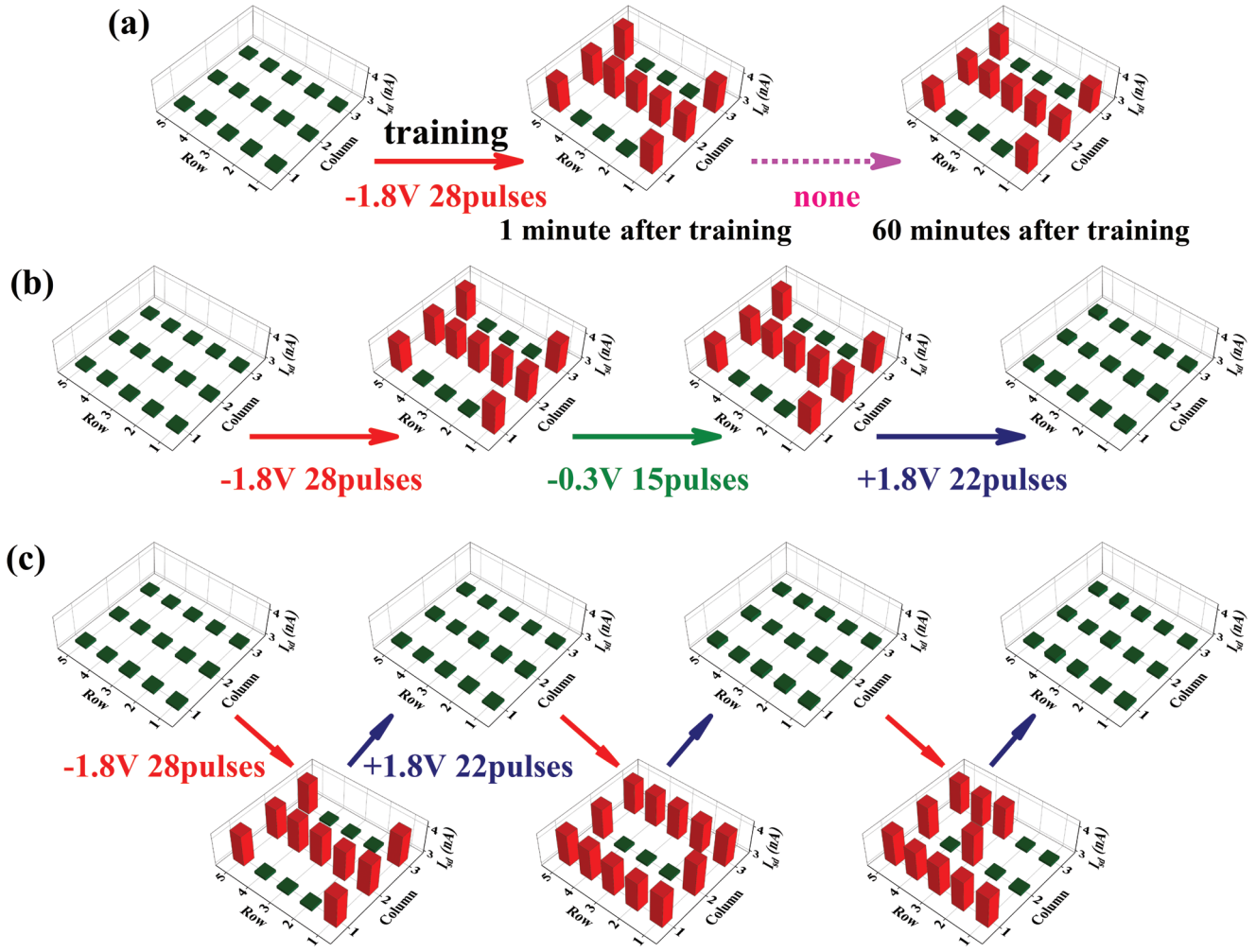

Figure 4. Strontium ferrite synapse array for image memorization. a) A 3 × 5 synapse array was implemented as a trainable memory. The image of "I" was input to the memory array using 28 pulses with –1.8 V amplitude (2 s duration, spaced by 4 s). These synapses exhibited long-term memory during the following hour, indicating electrolyte gating produces stable phase. b) The synapse memory is unaffected by spurious inputs (–0.3 V amplitude, 15 pulses with 2 s duration), showing good fault tolerance. The synapse array subsequently "forgets" after applying positive gate pulses (1.8 V amplitude, 22 pulses with 4 s duration). c) Images of the letters "I," "O," and "P" were successively programmed into and erased from the synapse array.

width) after writing the "I" pattern (–1.8 V amplitude, 2s width) (Figure 4b). The synapse array is sensitive to the writing pulses and is insensitive to the spurious pulses. After applying a spurious stimulus train with low bias, the temporal conductance enhancement immediately decays (Figure S11, Supporting Information). This short-term phenomenon can be understood in terms of an electrostatic effect.[24] The channel conductance can recover to its initial value when reverse train pulses are applied and the pattern "I" completely disappears, showing that these artificial synapses can be erased. In order to demonstrate the writing and erasing processes in a more intuitive way, images of the letters "I," "O," and "P" were successively programmed into the synapse array by applying facilitating and depressing pulses (Figure 4c). The color level expresses the variation of the channel conductance after applying the pulse train. The above experimental results show that the electrolyte-gated SFO transistor emulates a biological synapse, which highlights the novelty of this material system for developing neuromorphic devices.

We further simulated the performance of an artificial neural network using the experimentally measured conductance states (Figure 3d) for training with back-propagation of two data sets: a small image version (8 × 8 pixels) of handwritten digits from the "Optical Recognition of Handwritten Digits" dataset[49] and a large image version (28 × 28 pixels) of handwritten digits from the "Modified National Institute of Standards and Technology" (MNIST) dataset.[50] A simple three-layer network (one hidden layer) was utilized in our simulations using CrossSim[51] simulator as shown in **Figure 5**a. The schematic in Figure 5b shows a crossbar array of a synaptic weight layer. Here, the crossbar, regarded as part of a "neural core," performs vector-matrix multiplication and outer-product update operations.[4,52] The cumulative distribution functions during potentiation and depression processes are plotted in Figure S12 in the Supporting Information. Figure 5c,d shows the results of training a neural network using ferrite synaptic transistors, along with simulations of the ideal floating-point-based neural network performance, which provides a theoretical limit

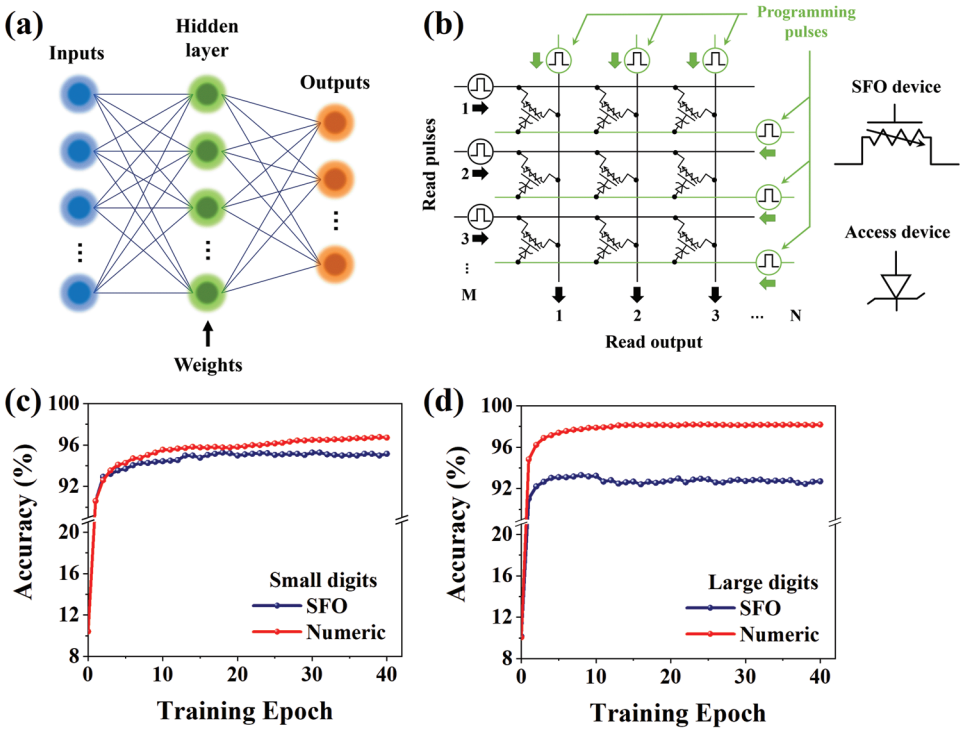

Figure 5. Image recognition simulations with various device parameters. a) Schematic of a three layer neural network. b) Schematics of showing hardware implementation with a synaptic layer composed of electrolyte-gated transistor crossbar array and access devices. c,d) Evolution of accuracy with training epochs for small digits (c) and large digits (d) with an ideal device and a ferrite synaptic transistor.

for the algorithm. For small digits, the classification accuracy approaches 90.6% within the second training epoch and approaches 95.2% after 16 training epochs (Figure 5c). One should note that 96.7% is the theoretical limit of ideal numeric training for small digits. For large digits, our simulations show that the neural network with ferrite synaptic transistors can provide classification with 92.7% accuracy (Figure 5d). The recognition accuracy is slightly lower than that with several recent synaptic devices.[52,53] However, the accuracy is much higher than that obtained with two-terminal resistive memory (20–70%) and phase-change memory devices (82.2%).[54] The key for improving the recognition accuracy is the linearity and symmetry of the potentiation and depression processes.[52] Further material and device improvements in this synaptic transistor are still required to reach higher recognition accuracy.

In summary, we presented a novel three-terminal synaptic transistor that uses SFO, a topotactic phase transformation material. The transition between the BM and PV phases in the SFO films with an ILG was experimentally confirmed from XRD and STEM measurements. Switching between memory states was linked to switching between the insulating BM and conductive PV phases in the SFO films, which is attributed to oxygen ion insertion and extraction in the channel material during ILG. This artificial synapse in a three-terminal configuration can implement important synaptic functions, including synaptic plasticity and STDP. A simulated artificial neural network built from these ferrite synaptic transistors exhibits accurate (95.2%) classification of handwritten data. Topotactic phase transformations are inherently nonvolatile, reversible, and stable. The introduction of advanced topotactic phase transformation materials into synaptic transistors may facilitate the development of novel high-performance neuromorphic devices.

Experimental Section

Sample Preparation: Brownmillerite phase $SrFeO_{2.5}$ thin films with a thickness of 50 nm were epitaxially grown on (001) $SrTiO_3$ substrates (MTI Ltd.) using pulsed laser deposition (PLD) with a 308 nm XeCl excimer laser, an energy density of ≈2 J cm^{-2}, and a repletion rate of 2 Hz. SFO films were deposited at 750 °C in a flowing oxygen atmosphere of oxygen pressure 1×10^{-3} Pa and cooled down to room temperature at 30 °C min^{-1}. The deposition rate of SFO films was further calibrated by X-ray reflection (XRR).

Device Fabrication: The thin films were patterned into channels with a coplanar gate structure using standard photolithography and argon-ion etching. The channel size was 210 µm × 50 µm. The Pt layer was prepared via electron beam evaporation as electrodes. An overlayer of a hard-baked photoresist was used as an isolation layer to prevent electric leakage between gate and source electrodes. Then, the devices were annealed in an oxygen atmosphere at 250 °C for 5 min to enhance the contacts. The transistor device was completed by dropping an ionic liquid *N*,*N*-diethyl-*N*-(2-methoxyethyl)-*N*-methylammonium bis-(trifluoromethylsulphonyl)-imide on the channel and gate electrodes.

Sample Characterization: X-ray diffraction measurements were performed using a Rigaku SmartLab instrument. Optical transmittance spectra were taken in air at room temperature with spectrophotometers (Cary 5000 UV–vis–NIR, Agilent and Excalibur 3100, Varian). The atomic structures of SFO films were characterized by an ARM-200F (JEOL, Tokyo, Japan) scanning transmission electron microscope operated at 200 kV with a CEOS Cs corrector (CEOS GmbH, Heidelberg, Germany) to cope with the probe-forming objective spherical aberration. HAADF images were acquired at acceptance angles of 11–22 and 90–250 mrad,

respectively. The electron energy loss spectra experiments were carried out with a Gatan spectrometer attached to the TEM in the STEM mode operating at 200 kV.

Electrical Measurement: The electrical characteristics of the electrolyte-gated SFO devices were measured in a Lakeshore probe station with a Keithley 4200 semiconductor parameter analyzer at ambient conditions. The sweeping rate was ≈1 mV s^{-1} for the transfer curves. The measurements for the temperature-dependent resistance were performed with a Keithley 4200 semiconductor parameter analyzer in Lakeshore probe station.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

artificial synapses, complex oxides, electrolyte gating, synaptic transistors, topotactic transformations

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