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Electrolyte-Gated Synaptic Transistor with Oxygen Ions

He-Yi Huang, Chen Ge, Qing-Hua Zhang, Chang-Xiang Liu, Jian-Yu Du, Jian-Kun Li, Can Wang, Lin Gu, Guo-Zhen Yang, and Kui-Juan Jin**

Artificial synaptic devices are the essential hardware of neuromorphic computing systems, which can simultaneously perform signal processing and information storage between two neighboring artificial neurons. Emerging electrolyte-gated transistors have attracted much attention for efficient synaptic emulation by using an addition gate terminal. Here, an electrolyte-gated synaptic device based on the $SrCoO_x$ (SCO) films is proposed. It is demonstrated that the reversible modulation of SCO phase transforms the brownmillerite $SrCoO_{2.5}$ and perovskite $SrCoO_{3-\delta}$, through controlling the insertion and extraction of oxygen ions with electrolyte gating. Nonvolatile multilevel conduction states can be realized in the SCO films following this route. The synaptic functions such as the long-term potentiation and depression of synaptic weight, spike-timing-dependent plasticity, as well as spiking logic operations in the device are successfully mimicked. These results provide an alternative avenue for future neuromorphic devices via electrolyte-gated transistors with oxygen ions.

1. Introduction

Computers built on the von Neumann architecture are especially good at numerical calculations. However, this kind of computing architecture is not efficient in performing gigantic tasks, primarily because the storage and processing processes are separated from each other, referred to as the von Neumann bottleneck.[1,2] In order to improve computational performance, the "data-centric" artificial neural networks and machine learning algorithms are developed by simulating the functional structure of the human brain in hardware.[3] Because there are about 10^{15} synaptic parallel connection of 10^{11} neurons in the human brain, it performs better and more efficiently when it completes learning tasks and executes commands.[4,5] Synapses are the basic units for signal transmission and regulation in neural networks, which the strength of the connection between two neurons is measured by synaptic weight. Currently, the devices implementing artificial synaptic functions include two-terminal devices such as resistive random access memory (ReRAM),[6,7] phase change memory devices (PCM),[8,9] magnetoresistive random access memory (MRAM),[10,11] and three-terminal devices such as electrolyte-gated three terminal transistors,[5,12–14] and ferroelectric field effect transistor (FeFET).[15,16]

The electrolyte-gated transistors give a flexible way for synaptic mimic.[5] The gate electrode can be regarded as the presynaptic neuron, and the channel between the source and drain can be regarded as the postsynaptic neuron. The conductance of the channel can be used to mimic the synaptic weight, which is an essential property in biological synapse. When the voltage pulses are applied to the gate terminal, it will set up an electric double layer at the interface between the channel and electrolyte, and then produce a huge electric field.[17] Under the huge electric field, the ions (such as H^+/O^{2-}) could be inserted or extracted to form new phases of the channel material. This process is reversible and nonvolatile for the conductance change. This process naturally resembles the signal transmission in biological neurons. When an electric pulse stimulates the presynaptic neuron, the synaptic vesicle will release the neurotransmitter to the postsynaptic membrane via the synaptic gap. Subsequently, the neurotransmitter will combine with postsynaptic neuron and an electric signal will respond to the postsynaptic neuron.[18] Thus, the applied gate voltage could manipulate the conductance states of the channel. The tuning of the conductance states can be corresponding to synaptic weight plasticity, which is the essential function of learning and memory behaviors for the human brain.[19] In contrast to the two-terminal artificial synaptic devices, the three-terminal transistor synaptic devices work by integrating the learning process and the information transfer at the same time.[20] However, the most commonly studied electrolyte-gate synaptic transistors with H^+ ions are limited to retention properties with seconds to hours, hindering their applications in an artificial neural network trained offline.[21–24] This phenomenon is ascribed to that H^+ ions would gradually decay back to ionic liquids due to the concentration gradient.[25] To get electrolyte-gated synaptic transistors with good retention property, we

H.-Y. Huang, Prof. C. Ge, Prof. Q.-H. Zhang, C.-X. Liu, J.-Y. Du, Dr. J.-K. Li, Prof. C. Wang, Prof. L. Gu, Prof. G.-Z. Yang, Prof. K.-J. Jin
Beijing National Laboratory for Condensed Matter Physics
Institute of Physics
Chinese Academy of Sciences
Beijing 100190, China
E-mail: gechen@iphy.ac.cn; kjjin@iphy.ac.cn
H.-Y. Huang, Prof. C. Wang, Prof. K.-J. Jin
School of Physical Sciences
University of Chinese Academy of Science
Beijing 100049, China
Prof. C. Wang, Prof. K.-J. Jin
Songshan Lake Materials Laboratory
Dongguan 523808, China
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.201902702.

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designed a $SrCoO_x$ (SCO) based transistor with O^{2-} ions by using its phase transformation.[26]

The brownmillerite $SrCoO_{2.5}$ (BM-SCO) structure, which consists of alternating stacks of $[CoO_4]$-tetrahedral and $[CoO_6]$-octahedron layers with ordered oxygen vacancy channels in the [110] crystal direction, provides a model system for oxygen ion insertion and extraction.[27] Besides, the cobalt ions are multivalent such as the stable Co^{2+} or Co^{3+} and the active Co^{4+}, providing the possibility of reversible redox reaction for SCO.[28] Recently, researchers have demonstrated that BM-SCO, an antiferromagnetic insulator, can be electrically transformed to a ferromagnetic metal perovskite $SrCoO_{3-\delta}$ (PV-SCO) through electrolyte-gating.[26] All these properties of SCO offer good opportunities for designing artificial synaptic transistors.

In our work, we demonstrated an electrolyte-gated synaptic transistor working with oxygen ions. The principle of the synaptic transistor is based on controlling the channel conductance via the insertion and extraction of O^{2-} ions through electrolyte gating. We investigated the electrolyte gating induced phase transformation in SCO, combining in situ X-ray diffraction (XRD), scanning transmission electron microscopy (STEM), electron energy-loss spectra (EELS), X-ray absorption spectra (XAS), and electrical transport and magnetic measurement. Then, we realized the nonvolatile multilevel memory states, and emulated important synaptic functions such as the synaptic long-term potentiation (LTP), long-term depression (LTD), synaptic spike-timing-dependent plasticity (STDP), and spiking logic operations.

2. Results and Discussion

2.1. Reversible Manipulation of SCO by Ionic Liquid Gating

We deposited high-quality epitaxial BM-SCO films with a thickness of 40 nm on $(LaAlO_3)_{0.3}$-$(SrAl_{0.5}Ta_{0.5}O_3)_{0.7}$ (LSAT) (001) substrates by pulse laser deposition (PLD). More details about the film growth procedure can be found in the Experimental Section. The BM-SCO films were confirmed by the high-resolution scanning transmission electron microscopy (HRSTEM) (**Figure 1**a). The crystal structure of BM-SCO can be viewed as alternating stacks of oxygen tetrahedral $[CoO_4]$ and octahedral layers $[CoO_6]$, with two periodic distinctive Sr–Sr atomic distances (Figure 1b). After ionic liquid gating with negative

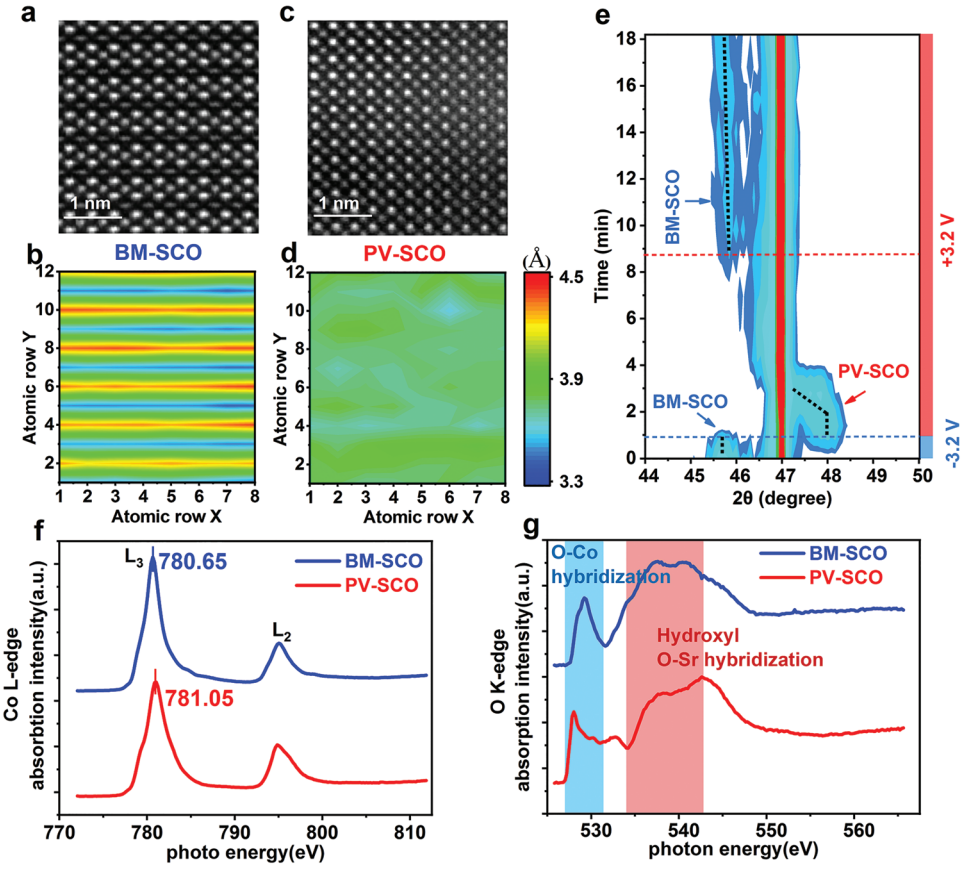

Figure 1. Phase transformation between BM-SCO and PV-SCO manipulated by ionic liquid gating. High-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) images of a) BM-SCO. b) Statistics of the Sr–Sr interatomic distances of BM-SCO. HAADF-STEM images of c) PV-SCO. d) Statistics of the Sr–Sr interatomic distances of PV-SCO. All the axis of STEM is along the [100] direction of the LSAT substrate. e) In situ XRD (θ–2θ) results around the LSAT (002) peaks. The BM-SCO to PV-SCO transition with the gating of –3.2 V while reversal PV-SCO to BM-SCO transition with the gating of +3.2 V, revealing a realization of a reversible electric field–controlled phase transformation between BM-SCO and PV-SCO. f) X-ray absorption spectra of Co $L_{2,3}$-edge for BM-SCO and PV-SCO films on LSAT, respectively. g) X-ray absorption spectra of the O–K edges.

voltage, the superstructure in BM-SCO changed to a perovskite (PV) structure consisting of octahedral layers [CoO_6] (Figure 1c,d). The results of high-resolution X-ray diffraction (XRD) and reciprocal space mapping (RSM) exhibit perfect crystalline quality of BM-SCO and PV-SCO (Figures S1 and S2, Supporting Information).

To prove the reversible phase transformation between BM-SCO and PV-SCO, we performed in situ XRD θ–2θ scans around the LSAT (002) reflection. Figure 1e illustrates the reversible phase transformation between BM and PV phases, with a negative gating of −3.2 V and a duration time of 50 s. The diffraction peak shifted from 45.7° to 48.0°, implying a phase transformation from BM-SCO to PV-SCO. If a positive voltage of +3.2 V is applied, a reverse phase transformation from PV-SCO to BM-SCO will occur. The in situ XRD experiment indicated the reversible control of SCO between BM and PV phases.

X-ray absorption spectroscopy measurements further proved the evolution of the electronic structure. The peak energy of Co L_3-edge shifts toward a higher energy from 780.65 eV of BM-SCO to 781.05 eV of PV-SCO (Figure 1f), indicating the increase of the Co valence state and the increase of oxygen stoichiometry by insertion. Moreover, the O *K*-edge of XAS shows that the Co–O peak hybridization intensity of PV-SCO is stronger than BM-SCO. Similar results can be obtained from the EELS measurements (Figure S3, Supporting Information).[27,28] The electrical transport properties of BM-SCO and PV-SCO were measured to explore the resistivity change during the phase transformation process. The results proved that the BM-SCO film is insulating and the PV-SCO film is metallic (Figure S4a, Supporting Information). It can be expected that the multistates of the electrical conductance for synaptic devices are produced during the phase transformation at room temperature. Furthermore, the change of electrical transport can be accompanied with the modulation of magnetism (Figure S4b, Supporting Information), enabling its potential application in magnetoelectric coupling devices.

2.2. Multilevel Conductance Modulation

We fabricated the electrolyte-gated transistor to simulate the biological synapses. The schematic illustration is shown in **Figure 2**a. More details about device fabrication can be found in the Experimental Section. Current–voltage (*I*–*V*) curves measured between the source and drain electrodes show good ohmic contact (Figure S5, Supporting Information). The ionic liquid N, *N*-diethyl-*N*-(2-methoxyethyl)-N-methylam-monium bis-(trifluoromethylsulphonyl)-imide (DEME-TFSI) was dropped on the channel and the gate electrodes as electrolyte-gated medium. The transfer curves of SCO transistors were measured by varying the gate voltage from 0 to −2.0 V, −2.0 to 2.0 V, and then back to 0 V with a sweeping rate of 5 mV s^{-1} at ambient conditions. A constant voltage (V_{SD} = 0.3 V) was applied between the source–drain electrodes. We simultaneously monitored the drain current (I_{SD}) and the gate leakage current (I_G) (Figure 2b). The transfer curves showed a clear large clockwise hysteresis loop, indicating the channel conductance could be reversibly manipulated between the high and low conductance states. When a negative voltage is applied on the gate electrodes, the electric field inside electric double layers induces the insertion of oxygen ions into the BM-SCO channel, evoking phase transformation from the low conductance BM-SCO to the high conductance PV-SCO. In contrast,

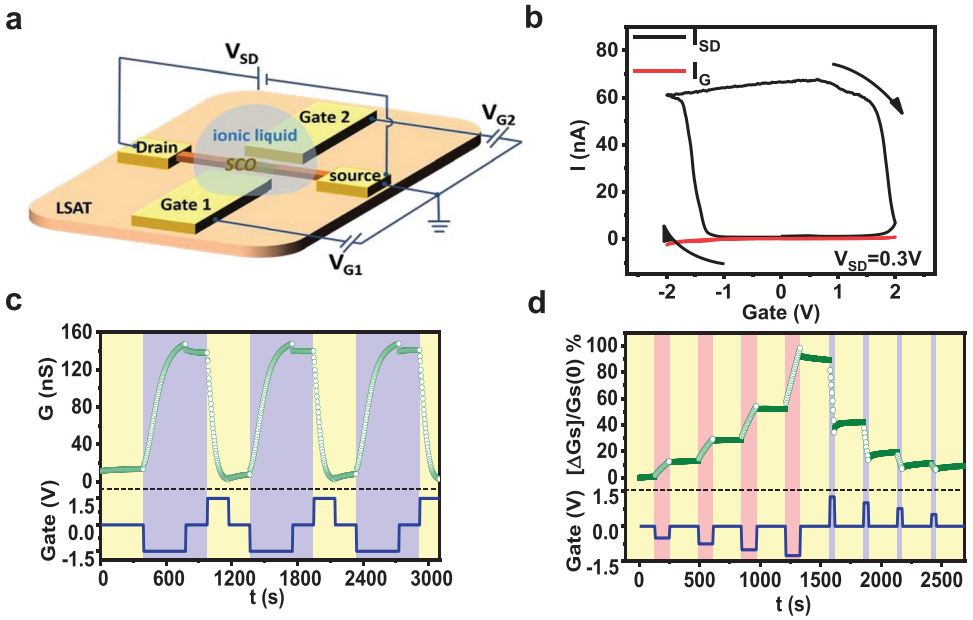

Figure 2. Structure and conductance modulation of three-terminal SCO transistor device. a) Schematic diagram of the three-terminal SCO synaptic device. b) The transfer curve of the SCO transistor. The source–drain current (I_{SD}) and the gate current (I_G) are shown as a function of gate voltage. The scan direction is indicated by the black arrows. c) The channel conductance modulation versus time under two gate voltages (–1.5 and 1.5 V) and the retention property under V_G = 0 V. d) The conductance change percentage versus time for 2 min pulses spaced 4 min apart with the negative voltage gate sequence –0.5, –0.75, –1, and –1.25 V, and 1 min pulse space 4 min apart with the positive voltage gate sequence 1.25, 1, 0.75, and 0.5 V.

positive gate voltages can induce the oxygen ions extracting from the channel, thus inducing phase transformation from PV-SCO to BM-SCO. The large hysteresis curve indicates the nonvolatile and reversible change of the SCO channel conductance that can be used for emulating synaptic functions. The nonvolatile dual-state memory behaviors of the SCO devices are shown in Figure 2c. At the beginning, we applied a voltage of 0 V for 400 s on the gate electrode. Then a gate voltage of –1.5 V for 360 s was applied on the gate electrode to increase the conductance from 13 to 120 nS. Subsequently, the device channel is stable at a high conductance state (120 nS) under gate voltage of 0 V. Then, a positive voltage of 1.5 V was applied to the gate for 180 s and the conductance returned to its original value (13 nS). By repeating the same gating sequence, we can obtain three cycles, demonstrating its repeatability. The multilevel conductance modulation is also available in the SCO devices (Figure 2d). Here, the 120 s pulses spaced 240 s apart of negative gate bias (in the sequence – 0.5, – 0.75, – 1.0, and – 1.25 V) and then 40 s pulses spaced 240 s apart of positive gate bias (in the sequence 1.25, 1.0, 0.75, and 0.5 V) were used for the gate modulation. In addition, we measured the retention properties of various conductance states for more than 3600 s (Figure S6, Supporting Information). This result further demonstrated good retention properties in the SCO based devices.

2.3. Synaptic Functions Emulated by SCO Transistors

In the three-terminal SCO transistors, the channel mimics a biological postsynaptic neuron and the gate electrode mimics a presynaptic neuron. The oxygen ions function as the neuron transmitters under the negative voltage gating, which can transmit information from the presynaptic neuron to the postsynaptic neuron. Since the ionic liquid contains an amount of trace water, the hydrolysis reaction will occur under high gate voltages. The required oxygen ions can come from this hydrolysis.[5,29] When a stimulus spike is applied on the presynaptic neuron, it triggers an excitatory postsynaptic current (EPSC) in the SCO channel. Long-term synaptic plasticity allows the brain to store a large amount of information, which is recognized as the biological basis of learning and memory activities at the cellular level.[30–32] As shown in **Figure 3**a, we recorded the EPSCs versus presynaptic spikes stimulation, which was induced by a series of gate voltage pulses with different amplitude (–0.2, – 0.4, – 0.6, – 0.8, – 1.0, – 1.2, – 1.4, – 1.6, – 1.8, and – 2.0 V) and the same duration time (10 s). The EPSC intensity increased with increasing the amplitude of spike voltages, and the retention value of the EPSCs can reach a maximum value up to 8.37 nA from the original state (3.67 nA). Moreover, the EPSCs had good retention property after 300 s. Long-term potentiation (LTP) is widely recognized as the basis for learning and memory in human brain.[30] We can realize the LTP process in the synaptic transistor by applying a series of positive voltage of presynaptic spikes (Figure 3b). The EPSCs triggered by a series of presynaptic spikes with different numbers (20, 40, and 60 pulses) and the same amplitude of voltage (–1.3 V for 5 s spaced 5 s apart). The EPSCs could be enhanced with increasing the pulse number. The maximum EPSC retention current increased 2 times compared with the initial state after applying 60 pulses for 1000 s. The synaptic weight can also be tuned by varying gate voltages with different amplitudes (Figure 3c). The EPSC retention current after 20 consecutive negative gate pulses (–1.8 V for 5 s spaced 5 s apart) increased by 10 times compared with its initial value. Thus, we can emulate the synaptic strength change by varying the spike number and amplitude. The above results imply that the SCO device can mimic LTP behavior of synapses. We applied the positive presynaptic spikes on the gate electrode to get a long-term depression behavior (Figure S7, Supporting Information). During LTP driven by negative gating, the electric field inside electric double layers tends to insert oxygen ions into the SCO channel, producing a transformation to more conductive states. The channel conduction will monotonically increase during LTP, because an increased number of negative pulses will intercalate more oxygen ions in the SCO channel. In contrast, positive gating tends to extract oxygen ions from the SCO channel, producing a transformation to less conductive states. Successive positive gate spikes will decrease the channel conduction by extracting more oxygen ions. Consequently, the potentiation and depression of synaptic weights can be emulated based on this principle. Combining the LTP and LTD processes, we applied 20 consecutive negative gate spikes (–1.4 V for 5 s spaced 10 s apart) and 11 consecutive positive gate spikes (1.4 V for 5 s spaced 10 s apart) to modulate the channel conductance (Figure 3d). The channel conductance increased by applying negative gate spikes (LTP), while the channel conductance decreased to the initial value (LTD) by applying positive gate spikes. Here, we demonstrated the 11 cycling LTP and LTD, indicating good repeatability.

Spike-timing dependent plasticity (STDP) is an essential function for the construction of a neural network. The function of STDP could be emulated by controlling the synaptic weights with the time-dependent spikes of presynaptic and postsynaptic.[33] Here, we realized the asymmetric and symmetric STDP functions (Figure 3e,f) in the SCO-based synaptic transistor. We used a multiplexer to convert the preneuron spikes and postneuron spikes to the gate voltage pulse outputs.[12] The waveform of the preneuron spikes and postneuron spikes can be found in Figure S8 of Supporting Information. For the asymmetric STDP simulation (Figure 3e), the strength of synaptic weight decreases when the postneuron spike is before the preneuron spike, meaning the $t_d < 0$. In contrast, the strength of synaptic weight increases when the preneuron spike is before the postneuron spike ($t_d > 0$). When the value of $|t_d|$ is large, the conductance change is smaller. We also achieved the symmetric STDP function (Figure 3f), by changing the shape of the spike waveform.

To further visualize the intrinsic long-term memory property in the SCO-based device, a 5 × 5 array consisting of SCO devices was employed for image recognizing and memorizing (**Figure 4**a). The letters "Y" and "X" were successfully memorized and erased under a series of gate pulses. In order to show the stimulus trains more clearly, three different types of the presynaptic pulse list (α, β, γ), which corresponds to the α, β, γ tag of pixels in the SCO synapse array, were shown in Figure 4b. The corresponding outputs of EPSCs were shown in Figure 4c. At the beginning, the three-terminal SCO synapses were arranged in a 5 × 5 array format with an initial conductance

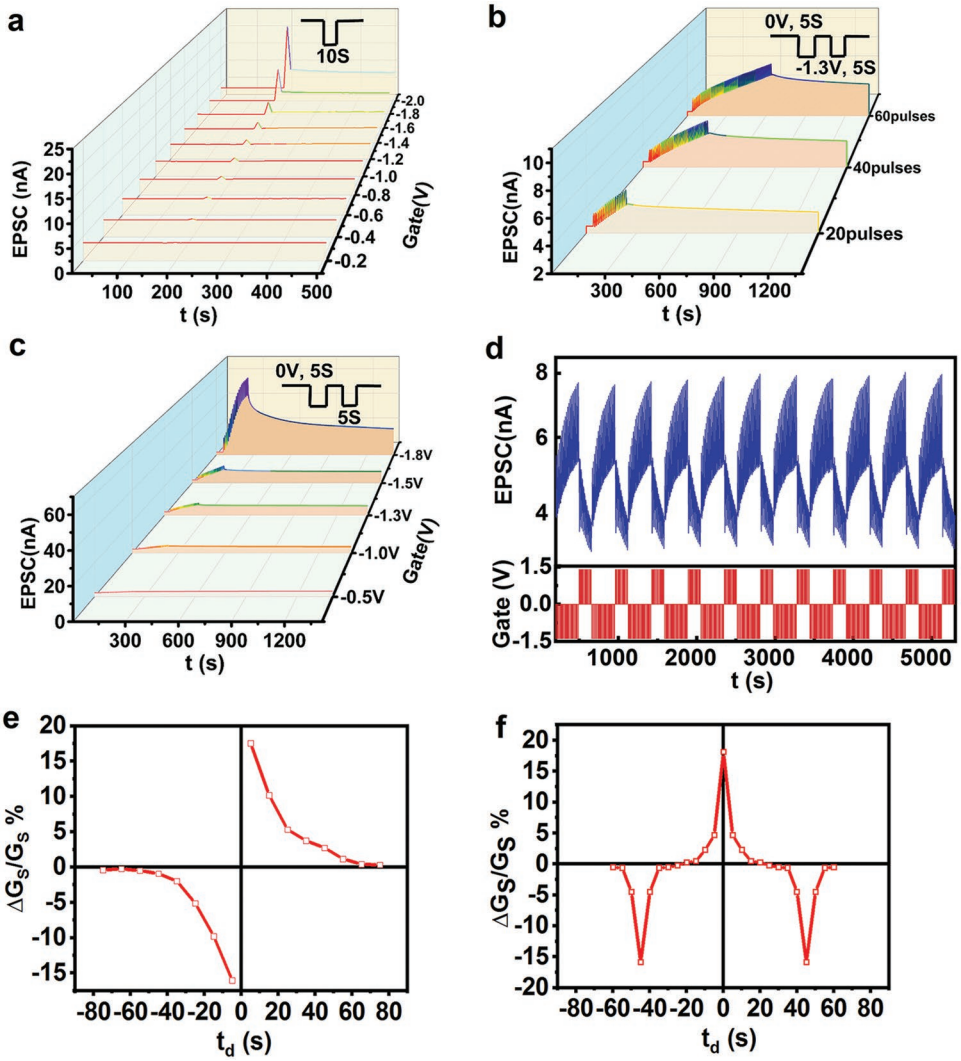

Figure 3. Synaptic functions emulated by the SCO devices. a) EPSCs stimulated by a series of the presynaptic spikes with different amplitude of voltages (–0.2, –0.4, –0.6, –0.8, –1.0, –1.2, –1.4, –1.6, –1.8, and –2.0 V) and the same duration time (10 s). b) EPSC stimulated by a series of pulses (20, 40, 60 spikes) with the same amplitude of voltage (–1.3 V). c) EPSCs stimulated by different amplitude voltage (–0.5, –1.0, –1.3, –1.5, –1.8 V) with the same 20 pulses (5 s duration spaced 5 s apart). d) Repeatability of synaptic long-term potentiation and depression. e) Asymmetric and f) symmetric spike-timing-dependent plasticity implemented in the SCO-based synapses.

state around the 3.6 nA (stage I). Subsequently, we trained the β and γ tag of pixels by applying 10 gate pulses (amplitude of –1.0 V, duration time of 5 s, time interval of 5 s). At the moment 50 s after the first 10 pulse training, a clear image of letter "Y" still remained in the synapse array (stage II), indicating the SCO-based synapses have good long-term memory property. Moreover, we trained the α and β tags of pixels by applying 10 gate pulses (amplitude of –0.5 V, duration time of 5 s, time interval of 5 s). Both of "X" and "Y" letters could be obvious in the synaptic array at the last pulse moment (stage III), while the letter "X" disappeared at the moment of 50 s after the last pulse (stage IV). The result proves that the long-term memory of the SCO-based transistor depends on the amplitude of the gate voltage. This phenomenon is ascribed to the requirement for the threshold value of the hydrolysis reaction.[5,26,34] Gate biases higher than the threshold value should be applied to dissociate the trace water inside ionic liquid, in order to inject oxygen ions by electrolyte gating. Besides, the synapse device has the ability of re-learning. We re-trained the β and γ tags of pixels by applying 10 pulses (amplitude of –1.0 V, duration time of 5 s, time interval of 5 s). Letter "Y" became more obvious at the moment of 100 s after the last pulse (stage V), demonstrating its good long-term plasticity. Finally, we erased the image of "Y" by applying 10 pulses (amplitude of 1.5 V, duration time of 5 s, time interval of 5 s). The moment of VI represents 50 s after the last training, and the channel current could recover to its initial value around 3.6 nA (stage: VI), indicating its capacity of forgetting.

The three-terminal SCO synaptic device could also be exploited to perform nonvolatile logic operations as shown in **Figure 5**. A schematic for the real device is shown in Figure 2a. The synaptic weights were manipulated by two in-plane

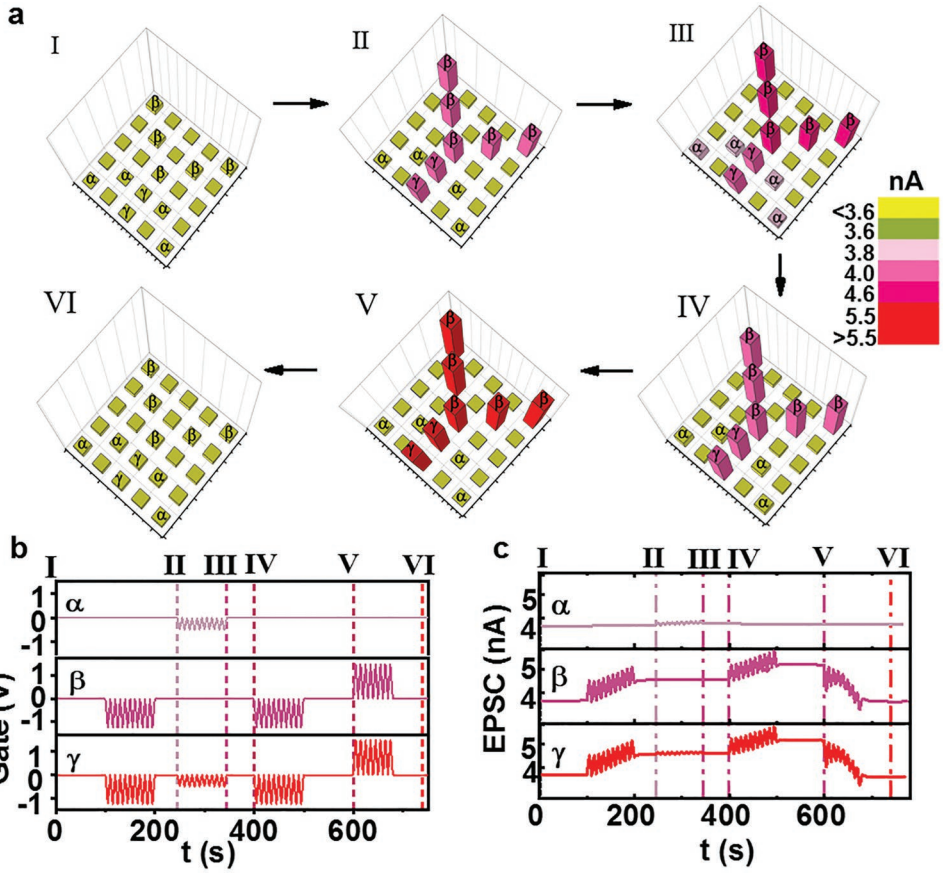

Figure 4. A 5 × 5 synapse array for pattern learning. a) Evolution of the channel currents (synaptic weights) during the learning and forgetting processes. Two letters ("X" and "Y") were chosen to illustrate short- and long-term memory, respectively. The initial states of the synapse array are in the low conductance state (*I*). Three different kinds of spike sequences (α, β, and γ) are presented on the gate electrode for mimicking the learning process. The resulting changes of I_{SD} are shown in II–VI, demonstrating the variation of synaptic weight at each pixel. b) A schematic of the three spike sequences used in (a). The marks I–VI indicate the corresponding moments of I–VI in (a). c) The EPSCs outputs corresponding to the pixel of α, β, and γ.

presynaptic Gate 1 and Gate 2 electrodes with the same electrode area. The output currents were measured by a constant source–drain voltage of 0.3 V. We defined the input voltage of 0 V as the logical "0" and the input voltage of −1 V with a duration of 20 s as the logical "1". When Gate 1 and Gate 2 input "00", the output current value was 3.7 nA. If Gate 1 and Gate 2 input "10", the output current value was 4.05 nA which remains approximately constant. Then, a positive voltage pulse of 1.2 V with a duration of 9 s was applied on Gate 1 to reset the channel conductance to its initial state (3.7 nA). If Gate 1 and Gate 2 input "01", the output current value was also 4.04 nA. On the other hand, provided that Gate 1 and Gate 2 input "11", the output current value was 5.5 nA and it was nonvolatile. When the threshold current is set as 5 nA, the output currents can exceed the threshold value only when both of the two gate inputs were present ("11"). Such behaviors are really resemblance to the logic "AND". If the threshold current is set as 4 nA, as long as any one of the gate spikes inputs is present (like "01", "10", "11"), the output current could exceed threshold value. Such behaviors are really resemblance to the logic "OR". The truth table of "AND" logical and "OR" logical is displayed in **Table 1**. It should be noted that the gate leakage current (≈10 pA) is about two orders of magnitude smaller than the channel current (≈nA), reflecting a negligible effect of the leakage current on logic operations. Thus we realized the "AND" and "OR" logical operations in the SCO-based synaptic transistors, which is important for computing function of neural networks.[35–37]

3. Conclusion

In summary, we demonstrated a three-terminal electrolyte-gated synaptic device based on the SCO films. The phase transformation between BM- and PV- phases of SCO films via oxygen ions by electrolyte gating was confirmed by XRD, STEM, XAS measurements. Multilevel conductance states can be produced by controlling the insertion and extraction of oxygen ions in the SCO films. Based on this working principle, we emulated various important synaptic functions such as long-term plasticity, STDP, and nonvolatile logic operations in our device. The results suggest electrolyte-gated synaptic transistor with oxygen ions could be a promising candidate for future neuromorphic hardware.

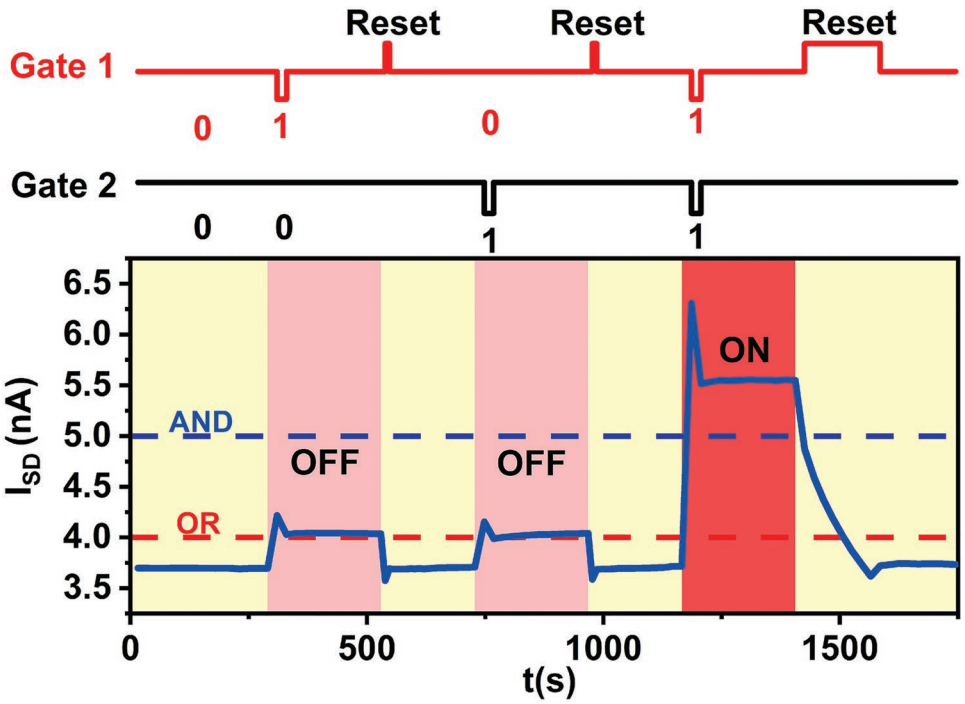

Figure 5. Digital logic Input list for a dual-gate synapse device (Gate 1 and Gate 2) and the output current curve. Here, the blue and red dash lines represent the threshold values of the "AND" and "OR" logics, respectively.

4. Experimental Section

Film Preparation: Epitaxial BM-SCO thin films (20–40 nm in thickness) were grown on $(LaAlO_3)_{0.3}$-$(SrAl_{0.5}Ta_{0.5}O_3)_{0.7}$ (LSAT) (001) substrates by pulsed laser deposition using a 308 nm XeCl excimer laser. The laser energy density was 1.2 J cm^{-2} and the repetition rare was 2 Hz. The films were grown at 750 °C under an oxygen pressure of 5 Pa.

Film Characterization: The XRD patterns of BM-SCO and PV-SCO films were characterized by a high-resolution four-circle X-ray diffractometer instrument (Rigaku, Smartlab). The atomic structures were investigated using the STEM (ARM-200CF, from JEOL) equipped with double spherical aberration (Cs) correctors, and the EELS measurements were carried out using a Gatan spectrometer attached to the TEM in the STEM mode. XAS of cobalt *L*-edges and oxygen *K*-edges was measured under high-vacuum level 6×10^{-7} Torr in synchrotron radiation facilities.

Device Fabrication: The SCO films were patterned into a transistor structure by standard microfabrication process. The channel size was 210 µm × 50 µm. The electrode of 5 nm Cr and 60 nm Au were deposited via thermal evaporation. Finally, the photoresist was spun on the device except the channel and the electrodes in order to decrease leakage current. The devices were annealed in a furnace under oxygen gas with a flowing rate of 20 mL min^{-1} at 250 °C for 5 min. Ionic liquid (DEME-TFSI) was dropped between the gate electrode and channel.

Table 1. The truth tables for the "AND" logic and "OR" logic.

Gate 1	Gate 2	AND [threshold 5 nA]	OR [threshold 4 nA]
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

Physical Properties Measurement: The electrical properties of SCO-based devices were measured using a probe station (Lakeshore) at the ambient conditions by a semiconductor parameter analyzer (Keithley 4200). The transport and magnetic properties were measured using physical properties measurement system (PPMS, Quantum Design Inc.). The temperature-dependent magnetization (M–T) was measured using field cooling mode with a magnetic field of 1000 Oe, and the magnetic field was applied along the in-plane direction of the film.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

artificial synapses, electrolyte gating, pulsed laser deposition, $SrCoO_x$, synaptic transistors

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