Experimental determination of interfacial-layer thickness from polarization-voltage hysteresis loops in $Pb(Zr_{0.4}Ti_{0.6})O_3$ thin films

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Interfacial layers near top and bottom electrodes with low resistivity in $Pb(Zr_{0.4}Ti_{0.6})O_3$ (PZT) thin film are identified and modeled through frequency-dependent polarization-voltage (*P-V*) hysteresis loops at frequencies below 20 kHz. Actual voltage drops, as well as built-in imprint voltage across the intrinsic ferroelectric layer, are found to be frequency dependent, as shown from the linear voltage shift of *P-V* hysteresis loops against applied external voltage at different frequencies with respect to one referenced hysteresis loop. Calculated interfacial-layer thickness is about 32±2 nm for an $Ir/IrO_2/PZT/Pt/SiO_2/Si$ capacitor with a PZT film thickness of 100 nm, in good agreement with the resistive measurements by Chu *et al.* [Appl. Phys. Lett. **81**, 5204 (2002)]. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1927270]

Fast response and long-term reliability of $Pb(Zr,Ti)O_3$ thin-film capacitors are important for the application of non-volatile ferroelectric random access memories (FeRAMs). Switching time of the capacitors at high electric fields can reach a few nanoseconds that is ideal for a computer operating at a high speed.[1] However, the coercive field for domain switching in the thin films is thickness dependent, and the switching time can slow down to a few microseconds under a reduced applied voltage.[2] This sets upward limit of film thickness for FeRAM application with unchanged logic read/write voltages. On the other hand, the possible existence of interfacial layers with low resistivity can also set a minimum thickness of functional ferroelectric thin films due to leakage current consideration. To overcome the film thickness limits, it is necessary to understand the underlying physics of the interfacial-layer importance on domain switching.

The coercive voltages in thin films determined from polarization-voltage (*P-V*) hysteresis loops are frequency dependent and well fitted by Ishibashi's power law $V_c \propto f^{\beta}$, in terms of limited speed of domain nucleation.[2,3] However, the coefficient β is variable as the frequency is below 100 kHz in the thin films. Since the duration of each voltage step—to make up one whole triangular wave form—is long enough for domain nucleation during performing *P-V* hysteresis loops at low frequencies, the actual voltage drop across ferroelectric domains at low frequencies due to the existence of low resistive interfacial layers is uncertain. The recent works of resistive measurements on $Pb(Zr,Ti)O_3$ thin films with various film thickness indicate near-interface regions with lower resistivity than that in the bulk,[4] in contrast to derivation of an intrinsic coercive voltage as a function of film thickness.[5] Furthermore, whether the built-in imprint voltage is dependent on the applied frequency is seldom addressed from the power-law derivation. Inevitably, both factors would be involved in deriving one genuine coercive voltage for domain switching from *P-V* hysteresis loops in ferroelectric thin films.

In this letter, we develop one method to evaluate frequency-dependent voltage drop across interfacial layers from *P-V* hysteresis loops as well as polarization-dependent resistivity near interfacial layers. This method is also useful in the characterization of a built-in imprint voltage during domain switching at different frequencies.

$Pb(Zr_{0.4}Ti_{0.6})O_3$ (PZT) thin films were fabricated by a sol-gel spin-coating technique on commercial platinized Si wafers.[6] The precursor solution was deposited on the substrates repetitively, and each layer was baked at 300 °C for 2 min. The total film was finally crystallized at 700 °C for 3 min with a films thickness of about 100 nm. The films were integrated into $Ir/IrO_2/PZT/Pt/Ti/SiO_2/Si$ capacitors with a top electrode area of 8.5×10^{-5} cm^2 deposited by magnetron sputtering. An IrO_2 buffer layer (~50 nm) was annealed at 600 °C for 1 min to protect against Ir diffusion into the film. *P-V* hysteresis loops were measured by using a Radiant Technologies Material Precision Analyzer with a triangular wave form of 3 V in the frequency range of 100 Hz–20 kHz at room temperature. Frequency dependence of the capacitance was characterized by a HP 4192A impedance analyzer with an ac amplitude of 0.05 V. The leakage current density (dependent of stressing time and voltage) in the capacitors—measured by a HP 4156A semiconductor parameter analyzer—falls into the range of 10^{-5}–10^{-6} A/cm^2 at ±3 V after 60 s.

Figure 1 shows frequency-dependent *P-V* hysteresis loops from 100 Hz to 10 kHz for the capacitor preset positively (related to the top electrode) and negatively, respectively. The presetting time for each loop is set as long as 180 s to obtain equilibrium. Note that the negative coercive voltage is obviously frequency dependent for the capacitor preset positively. In contrast, this frequency dependence of the coercive voltage is rather weak for the capacitor preset negatively. The different behaviors cannot be understood only from the limited speed of the domain nucleation model, as well as a simple voltage shift of the hysteresis loop due to the built-in imprint voltage in the capacitor with opposite polarization.

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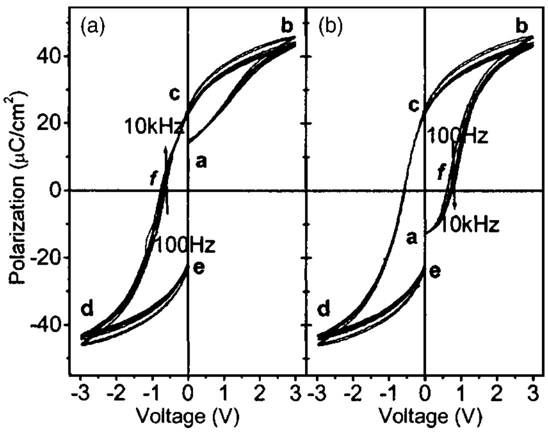

FIG. 1. Frequency-dependent *P*-*V* hysteresis loops for PZT capacitors preset (a) positively and (b) negatively.

To derive one actual voltage drop across ferroelectric domains at different frequencies, we calculate the voltage shift of *P*-*V* hysteresis loops at different frequencies as a function of applied voltage V_{appl} with respect to the *P*-*V* hysteresis loop at 100 Hz for the capacitor preset positively, as shown in Fig. 2. This method assumes that the speeds of domain nucleation and growth in our investigated frequency range are fast enough, so the frequency-dependent dielectric displacement in Fig. 1 can be regarded as the variation of actual applied voltage drop across the two discrete layers (one intrinsic ferroelectric layer and one interfacial layer) only. The voltage shift $\Delta V_i(f)$ has a linear dependence on the applied voltage at V_{appl}: $b \rightarrow c$ and $d \rightarrow e$, as shown in Fig. 2. All the lines intersect with one point to obey the following equation:

$$\Delta V_i(f) = k(f)(V_{appl} - V_0), \tag{1}$$

where V_0 is the induced voltage dependent of domain orientations, such as $V_0 = -0.23$ V at V_{appl}: $b \rightarrow c$, and $V_0 = 0.18$ V at V_{appl}: $d \rightarrow e$; and $k(f)$ is a coefficient of the slope

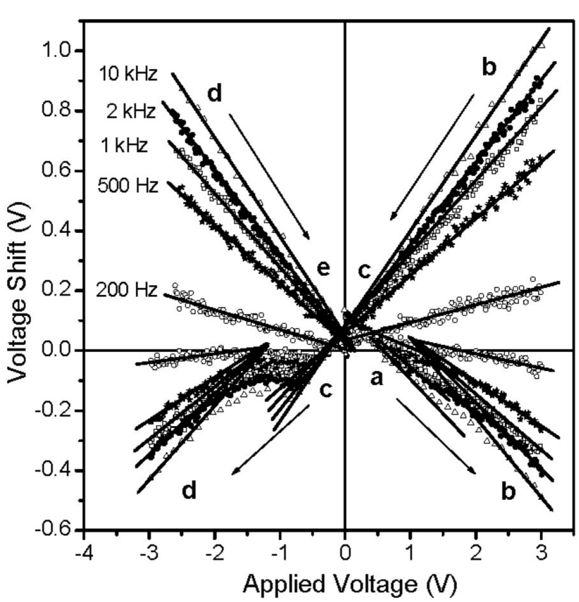

FIG. 2. Voltage shift of *P*-*V* hysteresis loops at different frequencies with respect to the loop at 100 Hz as a function of the applied voltage. Voltage cycling sequence is $a \rightarrow b \rightarrow c \rightarrow d \rightarrow e$, as shown in Fig. 1. The voltage shift at V_{appl}: $a \rightarrow b$ and $d \rightarrow e$ is reversed in the sign.

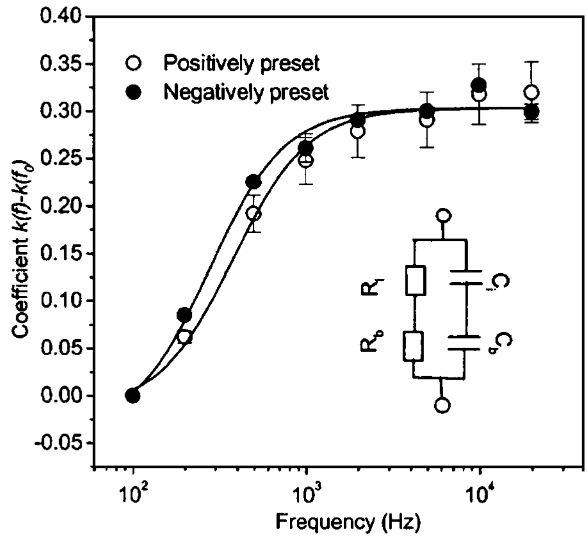

FIG. 3. Plot of coefficient $k(f)$-$k(f_0)$ ($f_0 = 100$ Hz) with respect to the frequency derived from line slopes in Fig. 2 at V_{appl}: $b \rightarrow c$. The solid lines are the best fitting of data [in accordance with Eq. (3)] for the capacitors preset oppositely. The inset shows one equivalent circuit for the total film.

increasing with enhanced frequency. Note that V_0 has a large negative voltage shift with decreasing applied voltage at V_{appl}: $c \rightarrow d$, as shown in Fig. 2. This is due to the imprint effect built up during domain switching that reduces the voltage drop across the interfacial layers.[7] As expected, the V_0 shift would disappear at V_{appl}: $a \rightarrow b$ for the capacitor preset positively. However, the shift still exists in Fig. 2, though it is much weaker than that at V_{appl}: $c \rightarrow d$. This suggests backward switching of a small portion of domains after polarization presetting in the capacitor.

During the crystallization of PZT thin films and thermal annealing of deposited electrodes after magnetron sputtering, the surface layers near electrodes are expected to be more conductive than the bulk due to the nonstoichiometric composition from PbO volatility and material interdiffusion between electrodes and film.[4] Therefore, we use one equivalent circuit to describe the whole system,[5] as shown by the inset in Fig. 3, where R_i and R_b ($R_b \gg R_i$) are resistors of interfacial and bulk layers, respectively, and C_i and C_b are corresponding capacitors. At high frequencies, the voltage drops acrossing individual layers are determined by C_i and C_b; under low frequencies, the voltage drops are decided by R_i and R_b instead. Therefore, we can calculate the voltage drop across the interfacial layers as follows:

$$\tilde{V}_i^*(f) = \frac{C_b}{C_b + C_i}\left[1 - \frac{1}{1 + 4\pi^2(C_b + C_i)^2 R_i^2 f^2}\right](V_{appl} - V_0) + V'(V_{appl}), \tag{2}$$

where $V'(V_{appl})$ is the voltage correction due to the Schottky barrier of electrode contacts.[8] In combination with Eq. (1), we have

$$k(f) - k(f_0) = A - \frac{B}{1 + Cf^2}, \tag{3}$$

where $A = (-1)^* k(f_0)$ ($f_0 = 100$ Hz), $B = C_b/(C_b + C_i)$, and $C = 4\pi^2(C_b + C_i)^2 R_i^2$. The fitted lines at V_{appl}: $b \rightarrow c$ are shown in Fig. 3, which gives $A = 0.303 \pm 0.008$, $B = 0.32 \pm 0.02$, and $C = 6.9 \pm 1.7 \times 10^{-6}$ s^2 for the capacitor preset positively; and $A = 0.303 \pm 0.002$, $B = 0.34 \pm 0.02$, and $C = 1.29 \pm 0.03$

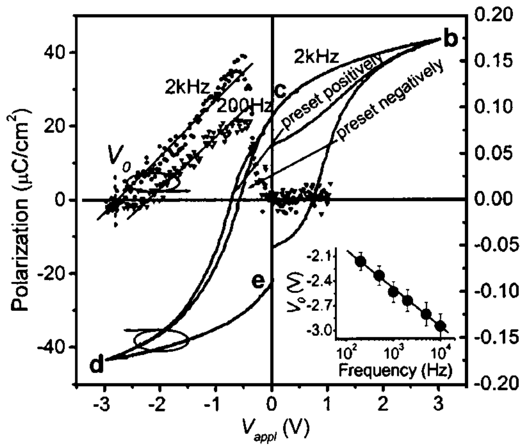

FIG. 4. *P-V* hysteresis loops, as well as their voltage shift, as a function of applied voltage at the same frequency for two capacitors preset oppositely. The inset shows derived V_0 as a function of the frequency.

$\times 10^{-6}$ s^2 for the capacitor preset negatively. If the dielectric permittivity of the interfacial layers is almost the same as that in the bulk, the corresponding interfacial-layer thicknesses are 32 ± 2 nm and 34 ± 2 nm. Within the experimental detection limit, the two values are nearly the same—independent of polarization orientation and close to 26 nm determined from resistive measurements.[4] The derivative interfacial-layer thickness does not change with branch selection of *P-V* hysteresis loops at different voltage regions, such as at $V_{\rm appl}$: $d\rightarrow e$, which indicates the validity of this method.

If two interfacial layers are regarded as back-to-back Schottky diodes under one external field due to electrode contacts,[8,9] the above calculated thickness for the total interfacial layers would be doubled. If the dielectric permittivity within interfacial layers is much smaller than that in the bulk, the calculated interfacial-layer thickness will be largely reduced otherwise. The resistivity within one interfacial layer is therefore estimated roughly as $4.5\times10^6\ \Omega$ cm and $2.0\times10^6\ \Omega$ cm derived from the fitted parameters B and C for the capacitor preset positively and negatively, respectively, which is much lower than the bulk resistivity in the range of 10^{10}–$10^{11}\ \Omega$ cm. The resistivity difference indicates polarization-dependent Schottky barrier.[9]

The interfacial-layer effect on the coercive voltage will become much weaker as the frequency is higher than 2 kHz, as shown by $k(f)$ plot in Fig. 3. However, the power law $V_c\sim f^{\beta}$ can be extended at frequencies of more than 1 MHz.[2] This suggests that another factor may become dominant at high frequencies. If the hysteresis loops for two capacitors—preset oppositely—are plotted together at the same frequency (Fig. 4), the loops at $V_{\rm appl}$: $b\rightarrow c$ and $d\rightarrow e$ are found to overlap completely except that the loops at $V_{\rm appl}$: $c\rightarrow d$ have one obvious difference. This difference is generally attributed to the polarization-dependent imprint voltage interpreted by the interfacial charge injection that shifts the *P-V* hysteresis loop.[7,10] However, the imprint voltage seems to be only important in the loop at $V_{\rm appl}$: $c\rightarrow d$ during domain switching, instead of the horizontal voltage shift of the total loop on the basis of this theory. Furthermore, the frequency dependence of negative coercive voltage is completely different for two capacitors preset oppositely, as shown in Figs. 1(a) and 1(b). If the loop difference at $V_{\rm appl}$: $c\rightarrow d$ (Fig. 4) is simply regarded as the voltage variation for domain switching due to their previous presetting histories, we derive another linear $\Delta V_i(f)-V_{\rm appl}$ plot to obey Eq. (1) under a voltage below -0.51 V at various frequencies. Unlike the plots in Fig. 2, $V_0(f)$ reflects that the frequency-dependent imprint effect changes more strongly with f, while $k(f)$ is nearly a constant, as shown by the inset in Fig. 4. The differences may be related to the dynamical development of the imprint effect at different frequencies during domain switching which is nevertheless much weaker at $V_{\rm appl}$: $b\rightarrow c$ or $d\rightarrow e$ without invoking domain switching. The derived negative coercive voltage for domain switching at various frequencies from *P-V* hysteresis loops is inevitably combined with the frequency-dependent imprint effect for the capacitor preset positively. The power law $V_c\sim f^{\beta}$ cannot truly reflect domain nucleation dynamics in thin films without debating this effect.

To summarize, the actual voltage drop across the intrinsic ferroelectric layer for domain switching in PZT is found to be frequency dependent. This is due to the existence of an interfacial layer and built-in imprint voltage. The imprint voltage seems to be only important during domain switching. The electrical circuit modeling gives the interfacial-layer thickness as well as resistivity. An interfacial-layer thickness of about 32 ± 2 nm for an $Ir/IrO_2/PZT/Pt/SiO_2/Si$ capacitor is estimated with a PZT thin film 100 nm thick. The power law $V_c\sim f^{\beta}$ determined from *P-V* hysteresis loops does not accurately predict the exact coercive voltage for domain switching in thin films without these considerations.

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