Temperature effect on carrier transport characteristics in $SrTiO_{3-\delta}$/Si *p-n* heterojunction

Haizhong Guo, Yanhong Huang, Kuijuan Jin, Qingli Zhou, Huibin Lu, Lifeng Liu, Yueliang Zhou, Bolin Cheng, and Zhenghao Chen[a)]
Beijing National Laboratory for Condensed Matter Physics, Institute of Physics, Chinese Academy of Sciences, P.O. Box 603, Beijing 10008, People's Republic of China

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A *p-n* junction has been fabricated by depositing an electron-doped (*n*-) $SrTiO_{3-\delta}$ film on a hole-doped (*p*-) Si substrate with a two atomic-layers thickness epitaxial SrO buffer layer using laser molecular beam epitaxy technique. Good crystallinity and smooth surface of $SrTiO_{3-\delta}$ were confirmed by reflection high-energy electron diffraction and x-ray diffraction. The junction shows good rectifying behavior at room temperature, and strong temperature dependence of current-voltage (*I-V*) properties in the range of 200–300 K. These results present potential applications in future microelectronic devices based on growing perovskite oxide thin films on conventional semiconductors. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1888039]

Perovskite-type oxide thin films are very attractive materials due to their simple crystal structures and multifunctional properties such as ferroelectric, dielectric, and optical properties. Epitaxial crystalline perovskite oxide thin films on silicon (Si) introduce the possibility for an entirely new device physics based on utilization of the anisotropic response of crystalline oxide films grown commensurately on a semiconductor.[1] Among the choices of perovskite oxide films epitaxially grown on silicon, $SrTiO_3$ (STO) is one of the most promising candidates, with desirable structure and dielectric properties.[1–3] Stoichiometric STO with Ti^{4+} ions has a d^0 electron configuration, and consequently is a insulator with a band gap of ~3.2 eV.[4] The electrical properties of STO can be changed from insulator to *n*-type semiconductor through reduction ($SrTiO_{3-\delta}$)[5–7] or impurity doping.[8,9] It is well known that *p-n* junction has been widely used as a basic element in various semiconductor devices. Compared to the conventional semiconductor *p-n* junctions, the ones of oxides could be expected to exhibit characteristics, such as magnetic behavior.[10,11] Moreover, oxide *p-n* junctions are expected to work at high temperature where the conventional semiconductor *p-n* junctions may not be competent. Along with the development of material fabrication technique, it is possible to prepare the artificially designed structures in view of integration with the mainstream microelectronic devices based on growing perovskite oxide thin films on conventional semiconductor, such as Si. However, there have been only a few reports on the fabrication of these artificially designed structures based on semiconductive perovskite oxide thin films on silicon.

In this work, we report the fabrication of a functional *p-n* heterojunction consisting of an *n*-type oxygen-deficient $SrTiO_{3-\delta}$ and *p*-type B-doped Si (*n*-$SrTiO_{3-\delta}$/*p*-Si) inserting a two atomic-layers thickness epitaxial SrO buffer layer. Good rectifying properties depending on temperature are found in the range of 200–300 K. Our results show that it is possible to realize rectifying junctions based on perovskite oxide thin films on conventional semiconductors.

$SrTiO_{3-\delta}$ film was deposited by laser molecular beam epitaxy (LMBE) technique equipped with *in situ* reflective high-energy electron diffraction (RHEED).[12] A Si (100) substrate (*p*-type, 12.95 Ω cm) was carefully cleaned sequentially using alcohol, acetone, and de-ionized water. Then, the substrate was dipped into HF (4%) solution for 30–40 s to remove the amorphous SiO_2 layer from the silicon surface, leaving a hydrogen-terminated surface. Subsequently, the Si substrate was immediately moved into the epitaxial chamber. The initial deposition of about two atomic layers of SrO film was under the base pressure of 5×10^{-6} Pa at the substrate temperature of 300 °C to prevent the formation of the SiO_2 interface layer. After that, the substrate temperature was raised to 620 °C. When the so treated SrO surface showed a sharp streaky RHEED pattern, the oxygen pressure was raised to 2×10^{-4} Pa. Then, a $SrTiO_{3-\delta}$ layer with a thickness of 150 Å was deposited. Finally, the sample was *in situ* annealed under the oxygen pressure of 2×10^{-4} Pa for 20

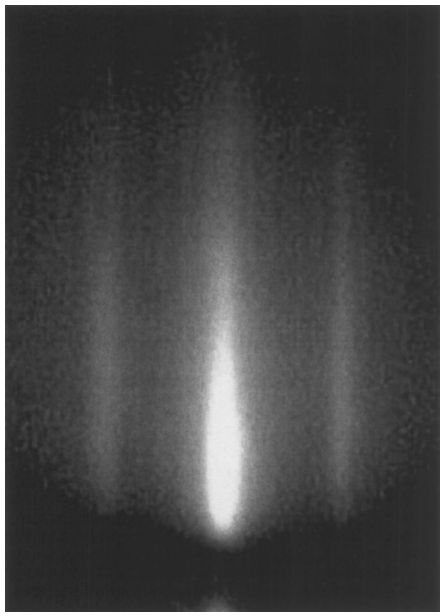

FIG. 1. RHEED pattern of the $SrTiO_{3-\delta}$ film with a thickness of 150 Å on Si (100) substrate at 620 °C under 2×10^{-4} Pa.

[a)]Author to whom correspondence should be addressed; electronic mail: zhchen@aphy.iphy.ac.cn

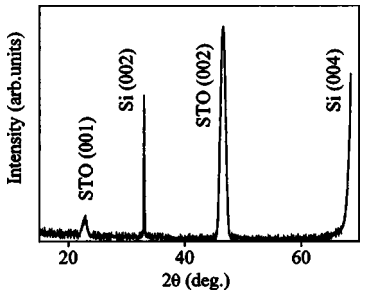

FIG. 2. XRD profile of the $SrTiO_{3-\delta}$ film prepared on Si (100) substrate.

min. The Hall coefficient measurement confirmed that the resistivity and carrier concentration of the $SrTiO_{3-\delta}$ film were 1.8×10^{-2} Ω cm and 4.83×10^{19} cm^{-3}, respectively.

The RHEED pattern of the STO film grown on Si substrate is shown in Fig. 1. The streaky and bright pattern clearly indicates the smooth STO surface and high degree of crystallinity of the film. X-ray diffraction (XRD) with Cu $K\alpha$ radiation was used to determine the phase structure. The XRD θ-2θ scan curve of the STO thin film is shown in Fig. 2. Except for STO (00ℓ) and Si (00ℓ) diffraction peaks, there are no diffraction peaks from impurity phases or randomly oriented grains. The full width at half maximum (FWHM) of the STO (002) peak is 0.87°, indicating a very high degree of crystallinity of the film.

The *I-V* behavior of the *n*-$SrTiO_{3-\delta}$/*p*-Si junction was measured by tuning the applied voltage in a wide range at room temperature, and the typical result is represented in Fig. 3. To obtain ohmic contact, indium (In) electrodes of 0.5 mm^2 were placed on the surface of $SrTiO_{3-\delta}$ and Si (inset of Fig. 3). The junction exhibits good rectifying behavior, and the shape of the *I-V* curve is similar to that of *p-n* diode made of conventional semiconductor. Even when −10 V was applied to the junction, the leakage current was as low as 10 μA. The threshold voltage (diffusion potential, V_D) is about 0.33 V; at that point the current starts to increase obviously as a result of the application of a positive bias voltage, as shown in Fig. 3. According to the band diagram description, V_D appears when a semiconductor is brought into contact with the other having a different carrier type or band structure.

The temperature dependence of *I-V* behaviors is shown in Fig. 4 measured in a wide temperature range of 200–300 K. The slope of the *I-V* curves shows more complex than that from the calculation of a conventional Si *p-n* diode.[13,14] In the $SrTiO_{3-\delta}$/Si junction, with increasing temperature, the

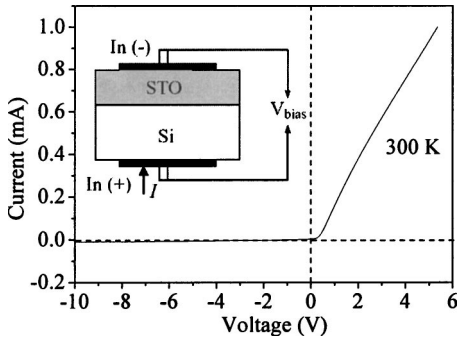

FIG. 3. The current-voltage (*I-V*) curve of $SrTiO_{3-\delta}$/Si junction measuring in a wide applied voltage scope at room temperature. The inset is the schematic structure of present *p-n* junction.

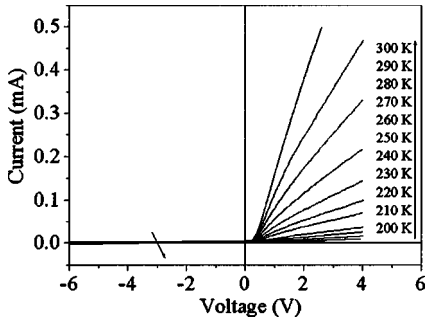

FIG. 4. The *I-V* curves of $SrTiO_{3-\delta}$/Si junction in a wide temperature range of 200–300 K.

slope of the *I-V* curve becomes clearly steeper in the forward bias side, and the threshold voltage (V_D) decreases nearly linear with temperature increasing. This phenomenon is quite different from that of the conventional Si *p-n* diode in which the shape of all the *I-V* curves is nearly independent of temperature in the forward direction.[15,16] In the reverse direction of Fig. 4, the leakage current saturates at $-I_s$, where I_s is the saturation current density. This is similar to the conventional Si *p-n* diode in which I_s slightly decreases with decreasing temperature.

Figure 5 shows the positive bias voltage dependence of the junction resistance at different temperature, defined as $R_j = dV/dI$. Obviously, with increasing the applied voltage, R_j decreases abruptly in low bias voltage range, but then almost tends to a constant when the applied voltage is larger than a certain value, the threshold voltage. Notice that the threshold voltage increases almost linearly with decreasing temperature, from 0.33 V at 300 K to 0.57 V at 200 K. It is very clear that the junction resistance increases with decreasing temperature.

To understand the above results, it is generally believed that the band model of semiconductor should be invoked. Figure 6 shows the schematic band diagram of the $SrTiO_{3-\delta}$/Si *p-n* structure. This simple model is based on continuity of the vacuum level, neglecting the effects of dipoles and interface states. The energy band profile is the case in which the electron affinity of Si is larger than that of STO. Therefore, a spike will occur in the conduction-band edges at the interface. Furthermore, the energy gaps of Si and $SrTiO_3$ are 1.12 and 3.2 eV, respectively, and that of $SrTiO_{3-\delta}$ is thought to be very close to $SrTiO_3$.[5] The work functions without doping in these two materials are regarded as 4.6 and 5.2 eV, respectively.[17] Carrier concentrations measured by Hall measurement are about 1.45×10^{15} cm^{-3} for Si and

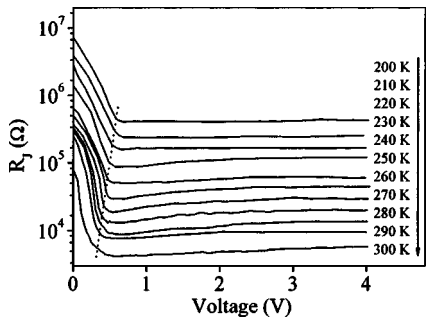

FIG. 5. The voltage dependence of junction conductive resistance at different temperature. The dotted line delineates the threshold voltage defined at that point the current obviously starts to increase.

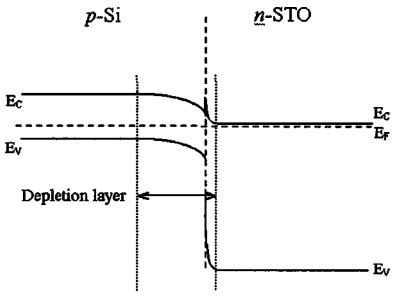

FIG. 6. Energy band diagram for $SrTiO_{3-\delta}$/Si junction.

4.83×10^{19} cm^{-3} for $SrTiO_{3-\delta}$. Thus the space charge region (depletion layer) is mainly located in the side of Si through the diffusion of carriers. According to the above parameters, we sketch the equilibrium energy band diagram.

With higher temperature, the carriers can be driven over the energy barrier at the $SrTiO_{3-\delta}$/Si interface by smaller applied voltage due to the Richardson effect. As temperature increases, the threshold voltage, V_D decreases; correspondingly, leakage current increases. Therefore the junction resistance decreases and the slope of *I-V* curve becomes steeper with increasing temperature as shown in Fig. 5. On the other hand, with increasing forward applied voltage, the potential of *n*-type STO increases relative to that of *p*-type Si. Therefore the height of the energy barrier decreases and the junction resistance decreases. When the applied voltage is larger than the threshold voltage, the barrier vanishes and the junction resistance tends to a constant.

In conclusion, a heteroepitaxial *p-n* junction was fabricated by depositing an oxygen-deficient $SrTiO_{3-\delta}$ on a *p*-type Si substrate with a two atomic-layers thickness epitaxial SrO buffer layer using LMBE. RHEED and XRD analysis demonstrated high quality heteroepitaxy of the *p-n* junction. The junction exhibits marked temperature dependence of its current-voltage (*I-V*) properties within the measuring temperature range of 200–300 K. The fabrication of a rectifying junction based on growing perovskite oxide thin films on conventional semiconductors might open up the possibilities in the future generation microelectronic devices.

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